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Article

Nearly Ideal WS_2 Schottky Diode with Asymmetric Gate Control Enabled by One-Side Edge Suspension

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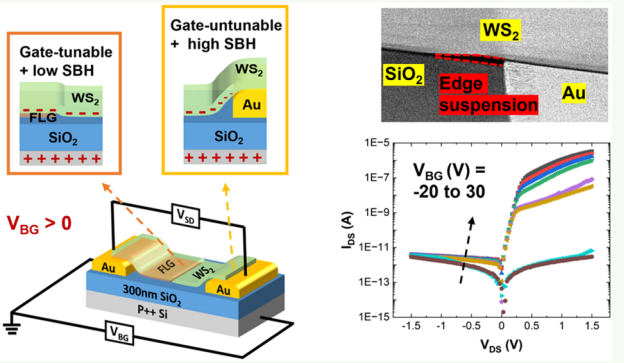
ABSTRACT: For two-dimensional materials (2DMs), challenges related to doping, contact, and structure engineering limit their practical implementation in basic electronic components, such as field-effect transistors (FETs) and diodes. A key issue is Fermi level pinning, which prevents the effective tuning of the Schottky barrier height (SBH). In this work, we propose an approach based on van der Waals stacking of multilayer WS_2 and few-layer graphene, incorporating a one-side edge suspension at the Au contact, which exhibits a high SBH. This design provides effective screening of the gate field, resulting in nearly ideal Schottky diode characteristics over the whole gate voltage sweeping window. Furthermore, our approach creates special asymmetric gate controllability between different drain-bias polarities, enabling unipolar gate modulation of forward-bias current while maintaining an ultralow reverse leakage at picoampere range. The one-side edge suspension design integrates functionalities of both the diode and FETs, revealing a promising application for 2DMs in areas such as current rectification and logic operations.



KEYWORDS: *two-dimensional material, field-effect transistors, diodes, Schottky barrier height, van der Waals stacking, asymmetric gate controllability, one-side edge suspension*

INTRODUCTION

Two-dimensional materials (2DMs), such as graphene and 2D transition metal dichalcogenides (TMDs), have great potential for next-generation applications. The reduced dimensionality of the 2DMs introduces exotic quantum properties and revamps designs and fabrications of electronic devices.[1,2] Among the 2DMs, semiconducting TMDs with moderate band gaps around 1−2 eV have advantages over the gapless graphene in logic applications, while possessing appropriate carrier mobility.[3] Functioning as channels in logic devices, the ultrathin TMDs allow extremely short channel lengths and improve device scaling, as well as power consumption, which are hardly achievable with conventional silicon semiconductors.[4]

Despite all of the attractions, fabrication of electronic devices based on 2DMs remains challenging. Due to the large surface/volume ratio, they are sensitive to device fabrication conditions. Formation of normal metal contacts to 2DMs could induce metal-induced gap states (MIGS) and interfacial defects, which cause severe Fermi level pinning (FLP) and considerable Schottky barrier height (SBH) independent of the metal work function.[5] The ability to tune SBH can be indispensable for realizing a broad range of electronic applications based on 2DMs. For example, to achieve high-performance TMDs FETs, the SBH should be minimized to reduce the contact resistance. In this regard, several approaches have been proposed, such as phase engineering of the TMDs channel beneath the contact[26,32] and FLP-free van der Waals (vdW) contact.[6−13] The latter approach also allows for the tunability of SBH by selecting the contact metal with different work function, which is crucial in designing a functional Schottky diode, in which a moderate SBH is the key to solving the issue of reverse leakage as well as maintaining the fast output switching.[14] There have been several reports regarding the Schottky diode devices made of 2D TMDs, in which versatile functions such as gate-tunable rectification,[15,16,28] photodetector,[17,27] and random-access memory[18] were presented. However, it is noteworthy that few of the reported devices simultaneously fulfill the key parameters of an ideal diode, including high forward conductance, ultralow reverse leakage current, that is, the current under reverse-bias voltage, and a unity ideality factor. For instance, the ideality factors of these diode devices usually deviate from unity, which can

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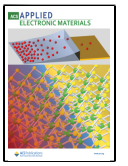

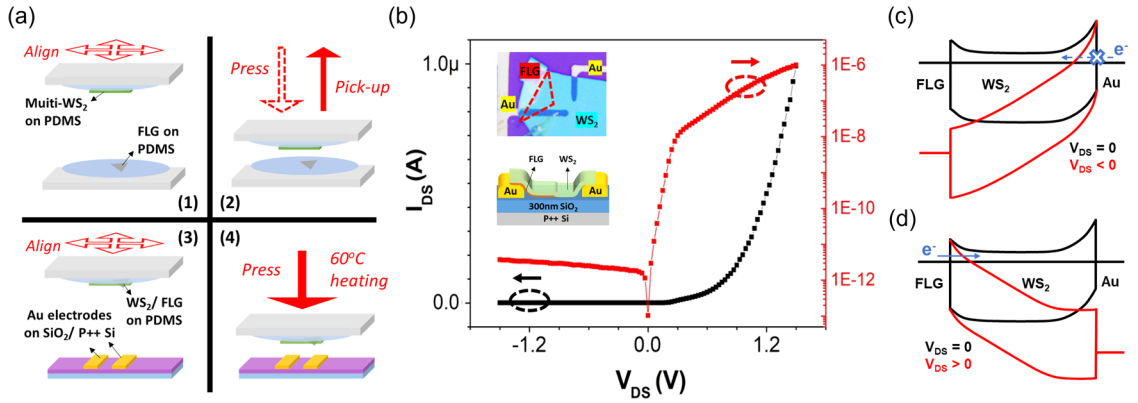

Figure 1. (a) Schematic of the deterministic vdW stacking process: (1) The multilayer WS_2 was aligned on the top PDMS to the FLG on the bottom PDMS. 2DMs here were prepared by exfoliation. (2) The aligned top/bottom PDMS was pressed to contact each other. Then, the FLG was picked up, forming a vdW assembly. (3) The vdW assembly was aligned on PDMS to the prepatterned Au electrodes. (4) The PDMS was pressed to the substrate. 60 °C heating was adopted to facilitate the transfer. (b) Output characteristic of the FLG/multilayer WS_2/ Au Schottky diode showing a decent diode behavior. Inset: OM image and schematic of the device structure. (c) Band diagrams of the device without and with reverse-bias ($V_{DS} < 0$). (d) Band diagrams of the device without and with forward-bias ($V_{DS} > 0$).

deteriorate the switching speed. Besides, the presence of electrical gating can readily influence the reverse leakage current, leading to a decreased rectification ratio and increased power consumption. Continued advancements in doping, contact, and structure engineering of 2D TMDs are essential for the reliable production of functional diode devices.

In this work, we present an approach for fabricating functional diode devices by using 2D TMDs. We started with a nearly ideal Schottky diode device comprised of thin multilayer WS_2, few-layer graphene (FLG), and prepatterned Au contacts through the deterministic vdW stacking technique,[19] which exhibited an exceptional rectification ratio exceeding 10^5, ideality factor approaching unity, and ultralow reverse leakage current in the picoampere range. In addition, it possessed an asymmetric gate controllability between the drain-bias (V_{DS}) polarities, with an on/off ratio $>10^6$ in the forward-bias region and completely free of gate modulation in the reverse-bias region. The intrinsic ideality of the diode device over the gate-sweeping window was carefully verified by the modified ideal diode equation, which separates the series resistance effect. A scanning electron microscope (SEM) revealed the suspension of the WS_2 channel near the prepatterned Au contact in the tilted angle, effectively screening off the gate field at the drain side and eliminating the gate modulation. Successful creation of a one-side edge suspension at the Au contact, combined with the high SBH feature enabled by vdW stacking, ensures the ideality of the diode characteristic under gating. Furthermore, unequal effective SBHs for source/drain contacts were extracted using a modified ideal diode equation and a thermionic emission equation and contributed to the diode feature. Finally, we applied the concept to CVD-grown monolayer (ML) WS_2, which is more technologically relevant for future logical application. By introducing PMMA as the supporting layer for the less-stiff ML WS_2 and creating different heights for the prepatterned source/drain contacts, asymmetric gate controllability was successfully realized in the ML device, showing a good rectification ratio of $>10^3$ and gate modulation of $>10^6$. We experimentally propose a promising design strategy for realizing current rectification functionalities combined with gate modulation in ultrathin 2DM-based devices.

EXPERIMENTAL SECTION

Substrate Preparation. P++ Si substrates covered with dry-oxidized SiO_2 were patterned by photolithography and subsequently metalized with 5 nm titanium and 30 nm gold by thermal evaporation, followed by a lift-off process with acetone and isopropyl. Before the transfer process, the patterned substrates would be further cleaned by ozone exposure for 1 h or by O_2 plasma treatment for 15 min.

Deterministic Dry-Transfer Process. FLG and multilayer WS_2 were exfoliated from HOPG and WS_2 crystals (2Dsemiconductor Co.) onto polydimethylsiloxane (PDMS) stamps using a Nitto blue tape. The deterministic stacking process is schematically depicted in Figure 1a. First, the chosen multilayer WS_2 and FLG flakes on individual PDMS were aligned and subsequently pressed to make both flakes contact by our customized transfer system. After detaching the PDMS stamps, the FLG flake was picked up by the WS_2 flake. The OM image of this FLG/WS_2 assembly on PDMS is shown in Figure S1a. The pick-up process could be done because the WS_2 flake possesses stronger adhesion to PDMS due to its larger contact area than that of the smaller FLG flake. This method efficiently produces a vdW interface free of residues by assembling two fresh cleavage surfaces and is reproducible. Finally, we transferred the FLG/WS_2 assembly onto the prepatterned Au electrodes on a SiO_2/ P++ Si substrate, by the same operation of alignment. In this step, the substrate was heated to 60 °C to facilitate detachment of the assembly from the PDMS stamp. Figure S1b shows the entire OM image of the transferred assembly, while the inset of Figure 1b provides a magnified view of the device under a test.

Wet-Transfer Process. PMMA 950 K/A4 (Sigma-Aldrich) was spin-coated onto the commercial WS_2 monolayer (ML) grown on sapphire with 2000 rpm/3 min and left in ambient for 2 h to volatilize the solvent. ML/PMMA was detached from sapphire by soaking 1 M NaOH for 1 h and then scooped to a beaker with D.I. water where it was fished out by the prepatterned substrate. Finally, the sample was baked 75 °C/1 h for fully drying the water. In this study, PMMA was not removed after the transfer process in order to serve as the supporting layer.

Electrical Measurement. All measurements were performed under a dark environment and under a pressure of 10^{-2} Torr in a Lake Shore cryogenic probe station equipped with a Keithley 2636B source meter.

Material Characterization. Raman spectroscopy was conducted in a confocal laser system with an excitation wavelength of 488 nm. FEI Inspect F50 SEM was used to acquire the tilted-angle images of the samples.

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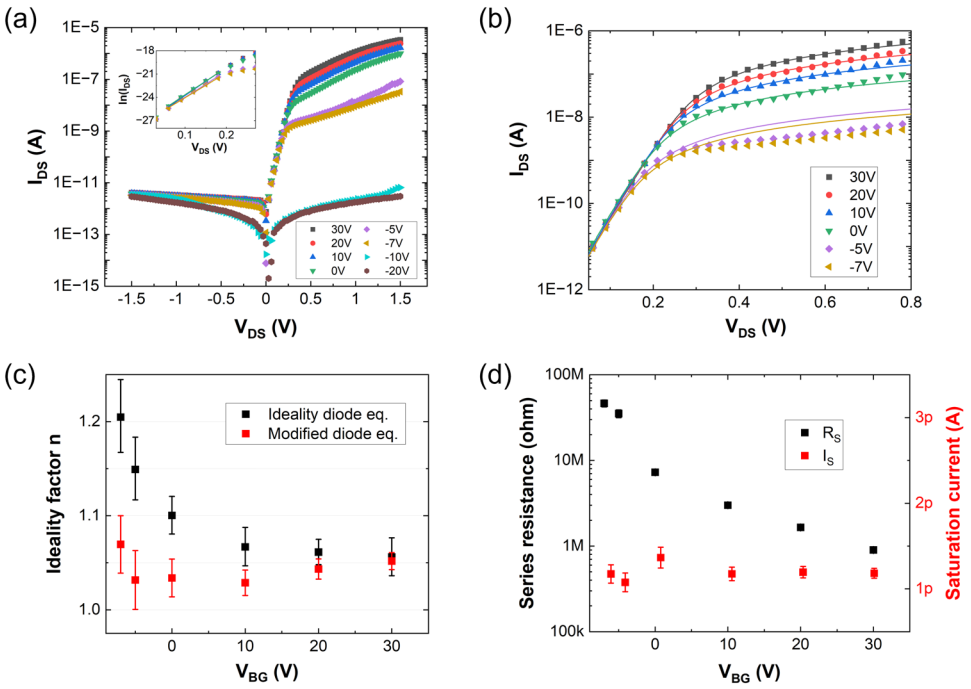

Figure 2. (a) Output characteristics under various V_{BG} conditions showing gate-dependent current rectification. Inset: $\ln(I_{DS}) - V_{DS}$ in a low forward-bias region. (b) Fitting the forward-bias region using the modified ideal diode equation. (c) Ideality factor n determined by an ideal/modified diode equation. (d) Series resistance and saturation current under various V_{BG} by fitting with a modified ideal diode equation.

RESULTS AND DISCUSSION

Figure 1b shows the output curve of the FLG/WS_2/ Au diode device, showing a decent diode characteristic. Following the conventional definition of a diode, forward- and reverse-bias regions are referred to as $V_{DS} > 0$ V and $V_{DS} < 0$ V. From the logarithmic plot, a large rectification ratio (>10^5) with $V_{DS} = \pm$ 1.5 V is observed. Such an asymmetric $I_{DS}-V_{DS}$ output curve could be obtained by depositing two kinds of metal with a significant work function difference for the source and drain contact, which requires steps of lithography and metal deposition on 2DMs.[20,21] In addition to the complexity of fabrication, such methods may be ineffective for 2D semiconductors because of the FLP issue, leading to the low rectification ratio despite the proper offset between the work function of metal and the affinity of 2D semiconductors. Besides, chemically reactive metals, such as Ti and Cr, are required to provide sufficient adhesion between substrates and noble metals.[29] These metals usually possess low work function and have strong tendency to hybridize with 2DMs.[26] The correspondingly reduced effective SBH could further deteriorate the rectification ratio in an n-type Schottky diode based on 2D TMDs.[28]

In our case, we created asymmetric contacts by precisely controlling the position in the transferring procedure, in which one electrode contacted the FLG flake, while the other one did not. The FLG flake could be viewed as an ultrathin insertion layer, which lowered the effective barrier height between Au and WS_2 considering its lower work function of ~4.6 eV[22] than Au of ~5.1 eV.[6] Under this scenario, the asymmetric contacts can be fabricated and exhibit characteristics of a diode without complex and detrimental processes, for example, two-step lithography and metallization. Given that the electron affinity of WS_2 is smaller than the work function of both FLG and Au,[6] unequal SBHs could form at the source and drain contact. Thus, our device should be viewed as a pair of back-to-back Schottky diodes with asymmetric SBHs. Accordingly, we sketch the band diagram of our diode device in Figure 1c,d, with unequal SBHs at both ends. When $V_{DS} < 0$ V, electrons are unable to pass the Au/WS_2 contact with larger SBH, attributing to the ultralow reverse leakage current. On the other hand, when $V_{DS} > 0$ V, electron injection from the FLG/WS_2 contact is allowed due to the lower SBH. Once the positive V_{DS} is large enough, depletion near the drain side, that is, the Au/WS_2 contact, can be canceled out, making the device highly conductive. Therefore, the Au/WS_2 contact serves as a Schottky diode providing good current rectification.

A gate-dependent diode characteristic was revealed by performing $I_{DS} - V_{DS}$ measurement with applying various back-gate voltage (V_{BG}), as shown in Figure 2a. Depending on V_{BG}, the forward-bias current could be either over 3-fold larger or several orders smaller compared to the case at $V_{BG} = 0$ V. An N-type FET characteristic was demonstrated with an on ($V_{BG} = 30$ V)/off ($V_{BG} = -20$ V) ratio exceeding 10^6 at $V_{DS} =$ 1.5 V. On the contrary, gate modulation in the reverse-bias region was limited within ~1.5 pA, negligible compared to the effectiveness in the forward-bias region. At low forward-bias ($V_{DS} < 0.2$ V), the curves corresponding to different V_{BG} are merged and exhibit similar upward slopes, except for those at $V_{BG} = -10$ and -20 V. At larger forward-bias ($V_{DS} > 0.2$ V), the merged curves become separate, in a sequence of the applied V_{BG}, and smoothly increase in parallel with each other. It suggests that gating only started to work when $V_{DS} > 0.2$ V, and a low reverse leakage current could be preserved under gating. The subtle difference between these merged curves was revealed through the calculation of ideality factor at each V_{BG}, which describes the steepness of linear fitting lines in the low forward-bias region. We performed linear fitting in a logarithmic scale in a low forward-bias region based on the ideal diode equation[23]:

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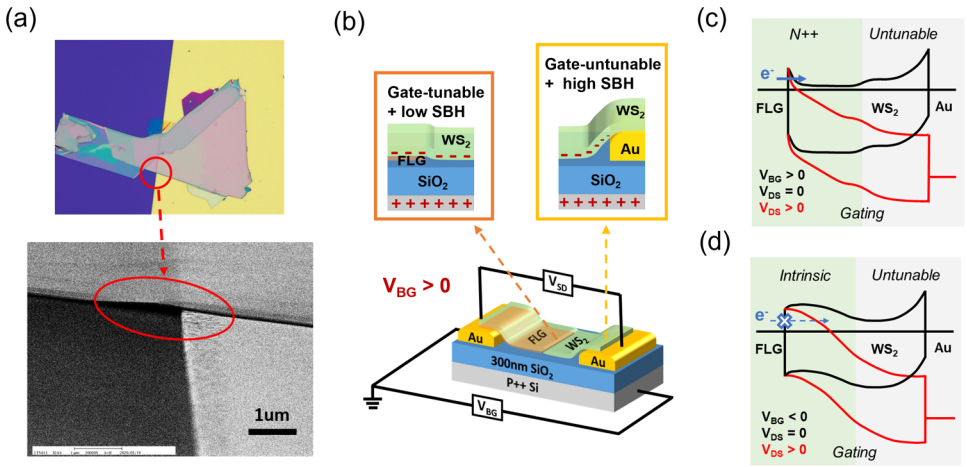

Figure 3. (a) OM (up) and tilted-angle SEM (down) images of the multilayer WS_2/Au contact. Suspension of the flake near the edge of Au electrode can be observed. (b) Schematic of the induced charges at the source (FLG/WS_2) and drain (Au/WS_2) contacts with unequal SBH under positive V_{BG}, as a result of asymmetric gate controllability. (c) Under positive V_{BG} and $V_{DS} > 0$, electrons can inject from the FLG contact with the thinned barrier width due to the increased carrier concentration. (d) Under negative V_{BG} and $V_{DS} > 0$, electrons are blocked at the FLG contact with the enlarged barrier height/width due to the reduced carrier concentration.

$$I_{DS} = I_s\left(\exp\left[\frac{V_{DS}}{nV_T}\right] - 1\right) \tag{1}$$

where I_S represents the saturation current over the Schottky barrier through thermionic emission, n represents the ideality factor, and V_T represents the thermal voltage, which is 25.85 mV at 300 K. The "−1" term is referred to as the contribution of reverse current flow, making the zero net current flow at equilibrium (V_{DS} = 0 V).

To eliminate the "−1" term, we started the fitting from V_{DS} = 60 mV. As shown in the inset of Figure 2a, the fitting results show high linearity, obeying the ideal diode equation. The values of ideality factor at different V_{BG} are shown in Figure 2c, which are gate-dependent and close to unity as V_{BG} becomes more positive. The best ideality factor achieved reaches ∼1.06. Though the device consisted of a pair of back-to-back Schottky diodes, the near-unity ideality factor suggested as if it was an ideal Schottky diode possessing only one metal/semiconductor interface. Theoretically, back-to-back Schottky diodes with a significant barrier difference at both ends, as we present here, can act as a single Schottky diode with the larger barrier under low forward-biased conditions.[24] Therefore, the ideality factor deduced here is in principle equal to the ideality factor of Au/WS_2 contact, which contributes to the overall diode characteristic.

Generally, the ideality factor may deviate from unity due to intrinsic causes like (1) onsets of different recombination mechanisms and (2) tunneling effects at reduced Schottky barrier height/width or extrinsic causes like series resistance effect, which could influence the "apparent" ideality factor. To verify if the diode is intrinsically unaffected by electrical gating, we need to rule out the influence of series resistance for precise evaluation of the ideality factor instead of the "apparent" ideality factor deduced by the conventional ideal diode equation. Thus, a modified ideality diode equation is introduced:[25]

$$I_{DS} = I_S\left(\exp\left[\frac{V_{DS} - R_S I_{DS}}{nV_T}\right] - 1\right) \tag{2}$$

where R_S represents the series resistance of the diode. Equation 2 describes a series connection of a diode and a resistor with a fixed series resistance R_S, which corresponds to the Au/WS_2 contact and the FLG/WS_2 contact in our device at one V_{BG}. Given that the FLG/WS_2 contact is gate-tunable while the Au/WS_2 diode is unaffected by gating, operating our device under various V_{BG} can be view as an identical diode connected to the different resistors in series, with each resistor corresponding to a specific V_{BG}. Since eq 2 is an implicit function, the zero-order Lambert W function is introduced to analytically solve the equation.[25] Thus, we have the following expression for eq 2:

$$I_{DS} = \frac{nV_T}{R_S}\text{Lambert } W_0\left[\frac{R_S I_S}{nV_T}\exp\left[\frac{(V_{DS} + R_S I_S)}{nV_T}\right]\right] - I_S \tag{3}$$

By fitting the output characteristics at different V_{BG} with eq 3, we acquire the ideality factor n, with excluding the influence of series resistance. Besides, we can obtain R_S and I_S at each V_{BG}. Here, I_{DS} and V_{DS} are the input parameters, and V_T is the only fixed parameter related to the temperature of the testing environment.

From Figure 2b, our data fit well with eq 3. We note some deviation occurs in the forward-bias region of the curves at V_{BG} = −5 and −7 V, which may be attributed to the excess series resistance effect close to the FET off-state. As shown in Figure 2c, the ideality factor extracted by the modified ideal diode equation is consistently below 1.07 at all V_{BG}. Note that for charge injection from a reverse-biased rectifying contact, electrical gating can modulate the effective barrier height because of the onset of tunneling effect at high carrier concentration, giving a large deviation of ideality factor from unity.[23] Our result suggests that the diode characteristic is robust under gating. The reason for the deviation of ideality factor is attributed to the additional voltage drop at the FLG/WS_2 contact, leading to the overestimated V_{DS} used in the ideal diode equation. In addition, R_S and I_S extracted from the fitting are shown in Figure 2d. While R_S values vary with V_{BG}, consistent with our prediction that high R_S occurs near FET off-state, I_S values remain fixed at a low level of ∼1 pA within the gate-sweep window. Since I_S can be directly correlated to

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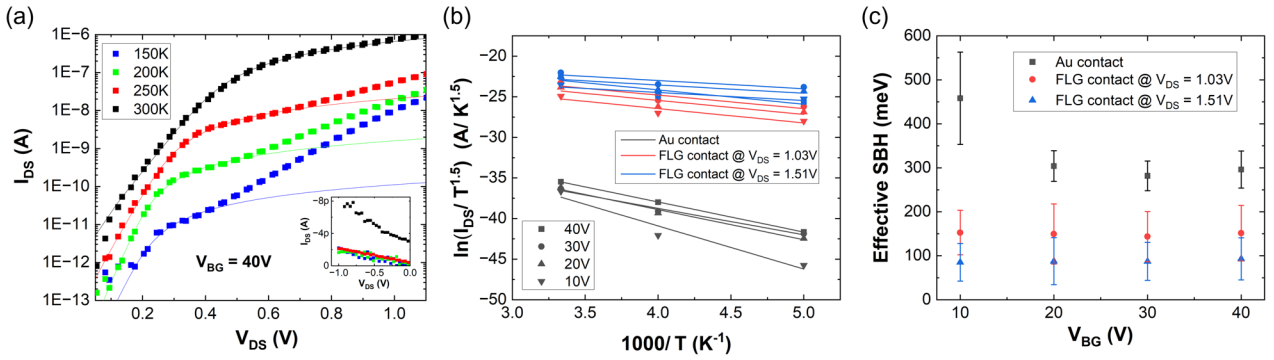

Figure 4. (a) Output characteristics under V_{BG} = 40 V at various temperatures. Solid lines are the fitting curves with a modified ideal diode equation. Inset: the reverse bias region, in which I_{DS} shows no temperature dependence. (b) Arrhenius plots of Au contact (V_{DS} < 0) and FLG contact (at V_{DS} = 1.03/1.51 V) under different V_{BG}. (c) Effective SBH versus V_{BG} as extracted from panel (b).

the effective barrier height at the M/S interface of Schottky diode according to the thermionic emission equation,[23] its independency with gating again indicates that the ideal diode characteristic of our device is well-preserved under gating. In Table S1, we benchmark our results against recent studies on lateral Schottky diode devices based on TMDs. Our device showed a very competitive rectification ratio and ideality factor. Furthermore, our device could exhibit a unique gate-independent nearly ideal diode characteristic, which has not yet been reported and discussed in other studies.

To reveal how the gate-independent ideal diode characteristic was realized, we carefully investigated the structure. Typically, Schottky contacts are sensitive to the applied gate voltage due to the relation between depletion width and electrostatic doping level.[26] The absence of gate modulation in the reverse-bias region implies that the electrical gating may be ineffective in the Au/WS_2 contact. Otherwise, the reverse leakage current should be enhanced. To figure out the reason, a multilayer WS_2 flake on an Au electrode was imaged by tilted-angle scanning electron microscope (SEM), as shown in Figure 3a. Instead of adhering closely to the edge of the electrode, around 2 μm wide flake areas are suspended. Only the top plane of the electrode forms a pure top contact. Figure 3b shows the configuration of electrical measurement and illustrates the asymmetric gating effect between both contacts at positive V_{BG}. For the Au/WS_2 contact with edge suspension, the electric field from the back gate is screened by the Au electrode, leading to the absence of induced charge, that is, no gate modulation. Combined with its high SBH, a nearly ideal and gate-untunable diode characteristic can be obtained. On the contrary, part of the FLG flake extends outside the Au electrode region and forms the FLG/WS_2 contact, eliminating the screening effect. With its low SBH nature, the FLG/WS_2 contact is efficiently gate-tunable. Therefore, asymmetric gate controllability is realized, that is, effective gate modulation at the source side and screening of gating at the drain side to maintain ultralow reverse leakage current. As the band diagram illustrated in Figure 3c, the source side, the FLG/WS_2 contact, as well as the channel region, can get electron doping with positive V_{BG}, while the drain side, the Au/WS_2 contact, keeps the same band bending due to the screening of gating. Consequently, the preserved Schottky barrier width at the drain side contributes to the consistently nearly ideal diode characteristic. On the other hand, electron doping near the source side can reduce the series resistance including the contact resistance and channel resistance, enhancing the diode characteristic by boosting the on-current level. Figure 3d shows the situation when negative V_{BG} is applied, in which the whole device becomes more intrinsic. It makes the effective SBH at the source side enlarged, which will block current flow. Accordingly, by adjusting V_{BG}, the device can be either turned "on" or "off", which refers to more conductive or open circuit.

To acquire the insight into the nature of asymmetric barrier height, the temperature-dependent IV measurement was performed. Figure 4a shows the output characteristics at different temperature with V_{DS} > 0 and V_{BG} = 40 V. Using eq 3, the fitted curves of output characteristics at different temperature are sketched, in which the reduction of simulated current levels at lower temperatures is observed. This can be attributed to the suppression of the thermionic emission current at lower temperature. As temperature reduces and V_{DS} increases, the dominating transport across the barrier at the source side can transit from thermionic emission to tunneling,[23] which has V_{DS} dependence, resulting in the deviation between the fitting curves and the experimental data. Note that eq 3 assumes that the device is composed of a diode and a resistor with fixed R_S. Once the actual R_S has V_{DS} dependence, the experimental data would deviate from the fitting result with R_S captured from fitting the low forward-bias region, where the voltage drop at the diode side is still dominant over the resistor side. As V_{DS} is large enough, the initially considerable built-in potential at the diode side is canceled out, and the voltage drop at the resistor side starts to increase.[24] This may explain why the experimental results at lower temperature can deviate from the fitted curves as V_{DS} increases, and I_{DS} at the high V_{DS} region exhibits weaker temperature dependence.

Temperature-dependent I_S data can be acquired for the cases with different V_{BG}. To determine the SBH for the diode, we put the I_S data into the Arrhenius plot based on the two-dimensional thermionic emission equation:[23,26]

$$I_S = AA^*T^{1.5}\exp\left(\frac{-e\varphi_B}{kT}\right) \tag{4}$$

$$\ln\left(\frac{I_S}{T^{1.5}}\right) = \ln(AA^*) - \frac{e\varphi_B}{kT} \tag{5}$$

where A is the contact area, A^* is the Richardson constant, and ϕ_B is the SBH.

Theoretically, I_{DS} at V_{DS} < 0 should be saturated to I_S, which is temperature-dependent. However, as shown in the inset of Figure 4a, I_{DS} remains at a similar level despite the difference in

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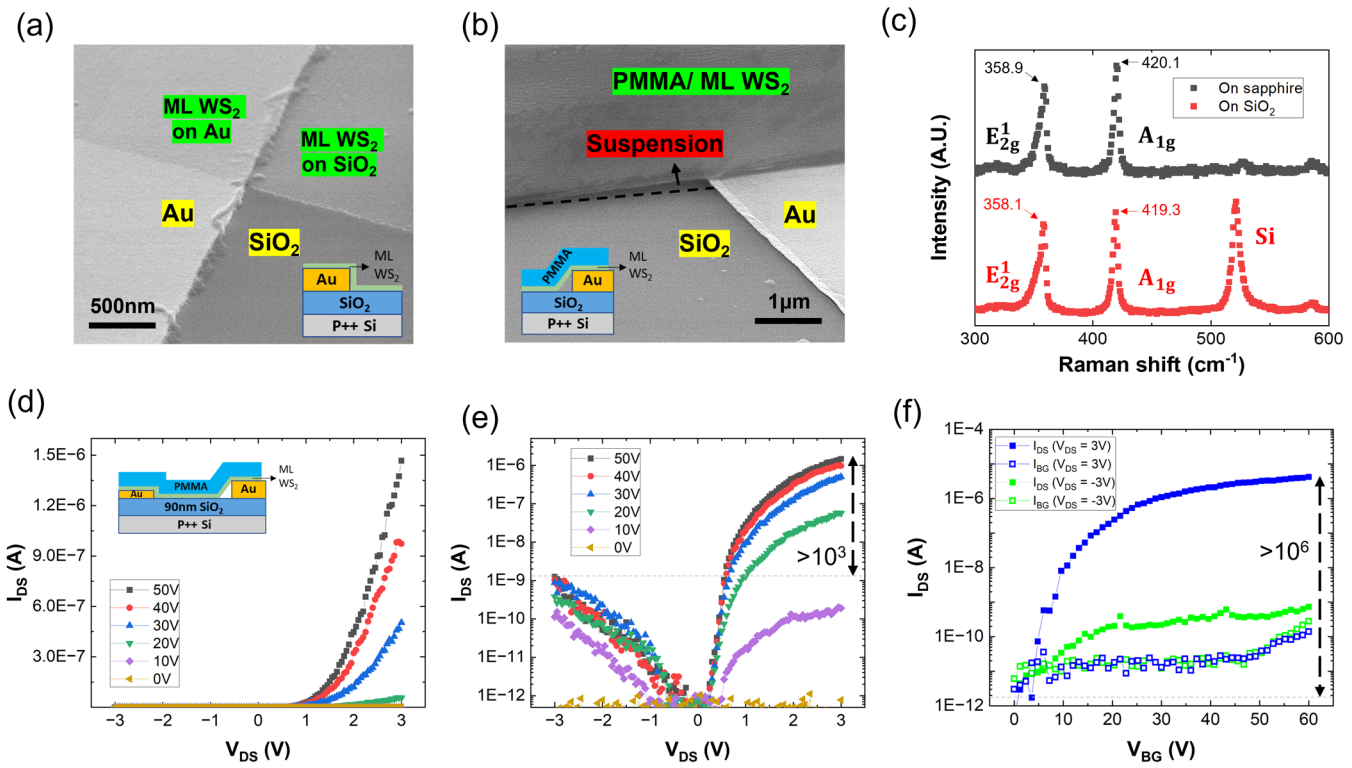

Figure 5. (a) Tilted-angle SEM image of CVD-grown ML WS_2 transferred onto a 40 nm Au electrode. (b) Tilted-angle SEM image of CVD-grown ML WS_2 with a PMMA-supporting layer transferred onto a 40 nm Au electrode. Suspension of PMMA/ML WS_2 at the contact edge is labeled. (c) Raman spectra of as-grown WS_2 ML on sapphire and after being transferred on a 90 nm SiO_2/P++ Si substrate with a PMMA-supporting layer. Peak positions are labeled and exhibit nearly no shifting after transferring. (d) Output characteristics in a linear scale, showing diode behavior. Inset: schematic of the device structure. (e) Output characteristics in a log scale, in which rectification ratio at $V_{DS} = \pm 3$ V can be $>10^3$ under $V_{BG} = 50$ V. (f) Transfer characteristics at $V_{DS} = \pm 3$ V, showing asymmetric gate controllability. At $V_{DS} = 3$ V, an FET on/off ratio of $>10^6$ is obtained.

temperature. This is possibly due to the limitation of noise level in our probe station.

As discussed above, charge injection at the high V_{DS} region will be dominated by the barrier at the source side. By taking the current value under specific V_{DS}, we acquire the effective SBH at these points, from the thermionic emission equation with a consideration of bias-dependent barrier:

$$I_{DS} = AA^*T^{1.5}\exp\left(\frac{-e\varphi_B'}{kT}\right) \quad (6)$$

$$\ln\left(\frac{I_{DS}}{T^{1.5}}\right) = \ln(AA^*) - \frac{e\varphi_B'}{kT} \quad (7)$$

where φ_B' is the effective SBH modified by the electrical bias across the barrier through the mechanisms of image force lowering[23] or bias-dependent work function.[30]

Figure 4b shows the Arrhenius plot for I_S and I_{DS} at V_{DS} = 1.03 and 1.51 V. Here, data extracted at 200, 250, and 300 K were used for analysis, as these temperature points provided a sufficient number of data points for reliable fitting. According to eqs 5 and 7, slopes of the linear fitting line indicate φ_B of the drain side and φ_B' of the source side at V_{DS} = 1.03 and 1.51 V, at different V_{BG}. The extracted values for barrier height from Figure 4b are plotted in Figure 4c, showing a significantly larger φ_B of the drain side over φ_B' of the source side. φ_B can be higher than 300 meV, effectively preventing the current flow under $V_{DS} < 0$ and contributing to the ultralow reverse leakage level. On the other hand, φ_B' is reduced from ∼150 meV at 1.03 V to below 100 meV at 1.51 V. This indicated that higher V_{DS} enhances tunneling currents across the source side barrier. An increase in the φ_B of the drain side is found at V_{BG} = 10 V. Such an increase in conventional situation can be attributed to the enlarged barrier due to the depletion above the flat-band condition induced by electrostatic doping.[26] However, considering the drain side in our device should be screened from gating due to the edge suspension, we argue that the increase may come from the depletion within the WS_2 channel, as the case shown in Figure 3d.

In the perspective of future electronic applications, ML TMDs enable better gate controllability and smaller device scale lengths. However, unlike bulk TMDs with high stiffness, ML TMDs are much softer and easily hang down when transferred onto a trench structure.[31] As shown in Figure 5a, in contrast to the multilayer case, ML WS_2 does not suspend but tightly adhere to the electrode step. Thus, a PMMA layer, the medium used in the wet-transferring process of ML WS_2, was intentionally kept in order to serve as a supporting layer. In Figure 5b, a suspension of the ML channel near the edge of the electrode is successfully created, which mimics the structure shown in Figure 3a. The Raman spectroscopy was conducted before (w/PMMA on growth sapphire) and after (w/PMMA on SiO_2 substrate) transferring. In Figure 5c, the Raman spectra exhibit no obvious change in peak intensity and position, whereas a newly observed peak at ∼520 cm^{-1} after transferring is the distinctive peak for silicon. Both the E_{2g}^1 and A_{1g} peaks of ML WS_2 exhibit a shifting of 0.8 cm^{-1} before and after transferring, suggesting that the ML channel remains

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intact and experiences negligible strain after the transferring process. To implement the PMMA-assisted design on the ML WS_2 channel, we fabricated asymmetric electrodes with different thicknesses. Au electrodes are 5nm/40 nm for the source/drain contact, accomplished through two-step photolithography and metal deposition. The thin electrode for the source contact allows the gate tuning of the effective SBH, while the thick drain contact electrode disables the gate modulation through one-side edge suspension. Figure 5d shows the output characteristics of the ML WS_2 diode under different V_{BG}, showing the gate-tunable current rectification effect. Further plotting the curves in a log scale in Figure 5e, we determine a rectification ratio $>10^3$ for V_{BG} = 50 V and V_{DS} = ± 3 V. In Figure 5f, the transfer characteristics at V_{DS} = 3 V exhibit an FET on/off ratio $>10^6$, while there is nearly no gate modulation at V_{DS} = −3 V. In Figure S2a−c, we show a bare ML WS_2 control device with 40 nm Au for the both source/drain contact. Obviously, without the aid of a PMMA-supporting layer to create the edge suspension, the device would have the same gate controllability at both contacts, resulting in a symmetric gate-dependent output characteristic, as shown in Figure S2b. In Figure S2c, the transfer characteristics at V_{DS} = 3 and −3 V are almost identical, suggesting the absence of an asymmetric gate control. We also fabricated an ML MoS_2 diode with the edge suspension structure, which also exhibited the asymmetric gate control between both V_{DS} polarities, as shown in Figure S3. Note that the slightly higher reverse current level may arise from the intrinsically smaller SBH of MoS_2 due to the FLP position near the conduction band edge.[5,6] To summarize, the experimental results indicate that our approach is reproducible and can be employed on different kinds of CVD-grown TMDs MLs, offering a good prototypical demonstration of a single electronic device capable of both current rectification and gate modulation.

CONCLUSIONS

We present a FLG/multilayer WS_2/ Au diode device, showing a high rectification ratio, near-unity ideality factor, and asymmetric gate controllability, which keeps ultralow reverse leakage despite varying V_{BG}. Screening of the gate field by the edge suspension at the high-SBH Au contact contributes to the preserved near ideal Schottky diode characteristic under gating. Implementing the concept of one-side suspension, the prototype device was demonstrated using CVD-grown ML WS_2 with a PMMA-supporting layer. Our experimental results demonstrate a promising design paradigm for integrating current rectification and gate modulation in ultrathin 2DM-based devices.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.5c00004.

OM images of FLG/WS_2 assembly on PDMS and the patterned substrate; device schematic and the output/transfer characteristics of the ML WS_2 control sample; summarized table for the performance of the lateral Schottky diodes based on TMDs; device schematic and the output/transfer characteristics of the ML MoS_2 diode (PDF)

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Notes

The authors declare no competing financial interest.

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