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Research Article

Ultralow Schottky Barriers in Hexagonal Boron Nitride-Encapsulated Monolayer WSe_2 Tunnel Field-Effect Transistors

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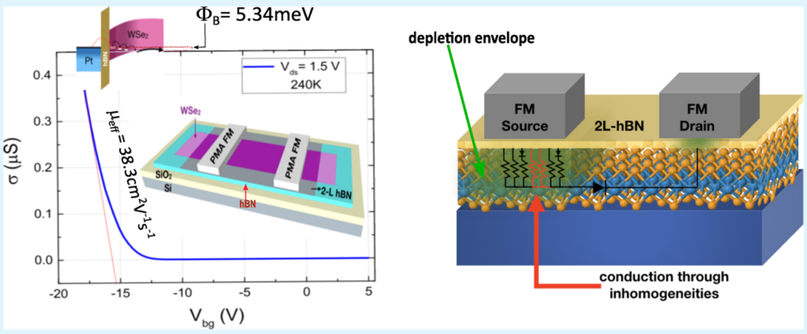

ABSTRACT: To explore the potential of field-effect transistors (FETs) based on monolayers (MLs) of the two-dimensional semiconducting channel (SC) for spintronics, the two most important issues are to ensure the formation of variable low-resistive tunnel ferromagnetic contacts (FCs) and to preserve intrinsic properties of the SC during fabrication. Large Schottky barriers lead to the formation of high resistive contacts, and methods adopted to control the barriers often alter the intrinsic properties of the SC. This work aims at addressing both issues in fully encapsulated ML WSe_2 FETs using bilayer hexagonal boron nitride (h-BN) as a tunnel barrier at the FC/SC interface. We investigate the electrical transport in ML WSe_2 FETs with the current-in-plane geometry that yields hole mobilities of ~38.3 $cm^2\ V^{-1}\ s^{-1}$ at 240 K and on/off ratios of the order of 10^7, limited by the contact regions. We have achieved an ultralow effective Schottky barrier (~5.34 meV) with an encapsulated tunneling device as opposed to a nonencapsulated device in which the barrier heights are considerably higher. These observations provide an insight into the electrical behavior of the FC/h-BN/SC/h-BN heterostructures, and such control over the barrier heights opens up the possibilities for WSe_2-based spintronic devices.

KEYWORDS: *monolayer WSe_2, ferromagnetic tunnel contacts, bilayer hexagonal boron nitride, field-effect hole mobility, BN encapsulation, Schottky barrier*

INTRODUCTION

A large number of two-dimensional (2D) materials, including graphene, hexagonal boron nitride (h-BN), transition metal dichalcogenides (TMDCs) such as MoS_2 and WSe_2, metal oxides (MxO_y), black phosphorene (b-P), and so forth, provide a wide range of properties and numerous feasible applications. On account of the potential in a wide range of applications in nanoscale devices such as logic circuits,[1] field-effect transistors (FETs),[2,3] light-emitting diodes,[4] ultrathin flexible devices,[5] photodetectors,[6,7] and so forth, 2D materials such as atomically thin TMDCs have been of significant interest to nano-electronics. In particular, single-layer TMDCs can be used in FETs as a high-mobility semiconductor channel,[8] resulting in significant on/off current ratios (I_{on}/I_{off} > 10^8)[9] and reduced power dissipation.[10] The coupled spin−valley physics[11] in TMDCs has also attracted broad attention in recent years as it provides a new opportunity for spin−(opto-) valleytronic applications[12] owing to the exotic effects arising from breaking of the inversion symmetry in monolayers (MLs) and strong spin−valley coupling. Besides these features, the atomically thin nature of 2D TMDCs is significant, in the sense that it allows for effective electrostatics to easily control carrier density in the channel by gate voltages because the thickness of the channel falls below the charge depletion region on the metal/TMDC interface. One of the excellent starting points for the development of high-performance digital electronic devices therefore is to comprehend the behavior

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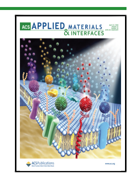

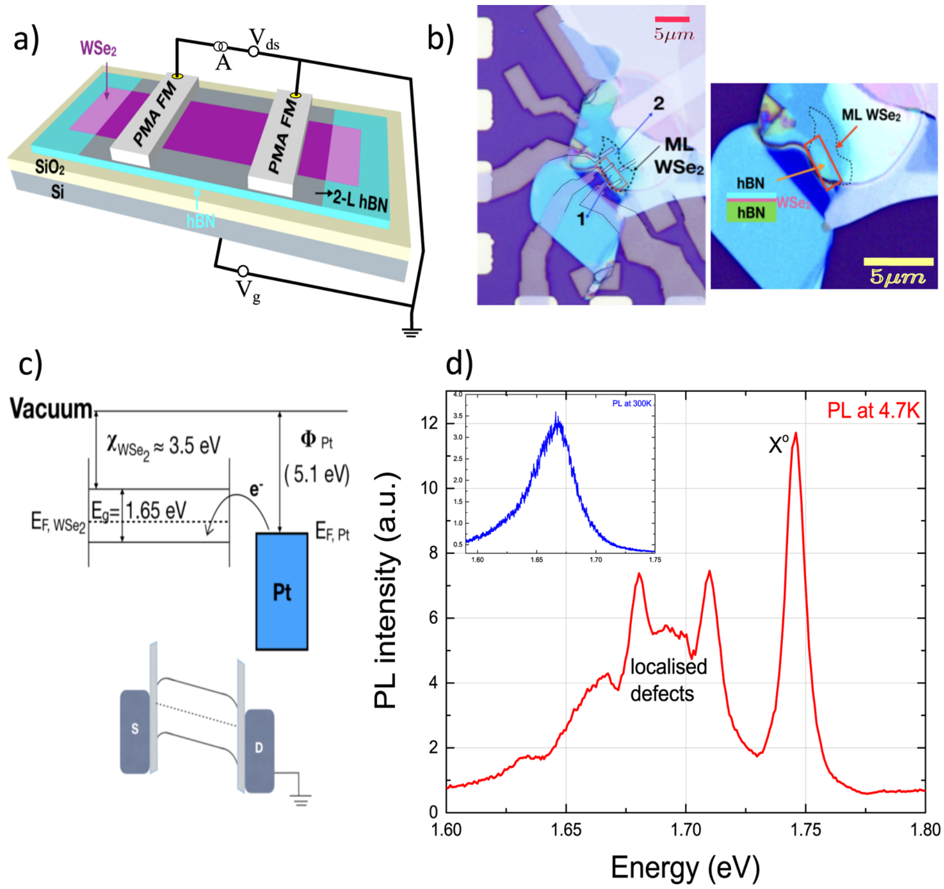

Figure 1. (a) Schematic of the h-BN-encapsulated ML WSe_2 tunneling device with FCs; (b) optical microscopy image of the device. The rectangular part (red) represents the encapsulated structure; the optical image of the encapsulated sample before defining contacts. (c) (Top) energy level diagram for ML WSe_2 with respect to the immediate contact material platinum; (bottom) schematic of the drain−source current under the forward bias condition under finite bias and over threshold gate voltage. Note that the majority charge carriers are holes in our devices. The band bending around the FCs is not scaled. (d) PL spectrograph for ML WSe_2 at 4.7 K (X° represents the neutral exciton peak); (inset) room temperature PL spectra for the same single layer of WSe_2 shows the single signature peak at 1.67 eV for collective excitations in a ML.

of the metal in contact with TMDCs.[13] Schottky contacts with low barrier heights (Φ_B) and low reverse leakage currents are key requirements in order to produce TMDC-based devices such as FETs that simultaneously preserves the intrinsic characteristics of the channel. This idea can also be extended to spin injection in these materials as long as there is a ferromagnetic (FM) contact[16] (FC) with a tunnel barrier such that the height of the overall barrier (FC/h-BN/SC) is low enough to enable optimization of values for contact and channel resistance. This is called the impedance matching phenomenon[17] and is a key element for injection and detection of spin in semiconductors.

Analysis of Schottky transistor's electrical characteristics at room temperature alone cannot provide a complete understanding of the mechanism of conduction and formation of barriers. However, temperature-dependent electrical behavior investigation may provide a detailed mechanism for current transport. To our knowledge, very little research in this direction of contact engineering for future lateral spin FET functionality has been made using FCs to ML TMDCs with an efficient tunnel barrier;[14−16] however, contacts with in-plane magnetization might be a bottleneck for fully electrical spin transport proposed in the MLs in this case because MLs of TMDCs prefer spin polarization in the *z*-direction originating from the Ising spin orbit coupling because of breaking of the mirror symmetry of the plane perpendicular to the 2d lattice plane,[18] despite the gate tunability of the barrier heights. Subsequent efforts were made to combine WS_2 with perpendicular anisotropic magnets with Al_2O_3 barriers, but even in this case, the Schottky barrier heights are considerably higher with the best value of 147 meV without any apparent gate tunability.[12]

This work focuses on the measurement and understanding of the gate-dependent and temperature-dependent charge transport properties in tunnel FETs formed by the ML of WSe_2 crystals with FM metal contacts with perpendicular magnetic anisotropy. Our findings show that a combination with a thin layer of h-BN on top of ML WSe_2 along with thick h-BN at the bottom not only allows for ultralow effective barrier heights but also allows this barrier height to be tuned with the gate voltages opening the possibility for modulation of these heights to yield comparable values for contact and channel resistance in the future for impedance matching and spin injection. The strategy of encapsulating allows for probing the intrinsic transport properties in the ML semiconducting channel (SC), while giving out the minimum effective Schottky barrier height as low as 5.34 meV using a 2D thermionic emission model[19] free from Fermi level pinning (FLP) effects. This tunability is manifestly lost in the unencapsulated device. For simplicity, here onward, we will refer the contact material

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as Pt, the part of the superstructure which is in immediate contact with bilayer h-BN and ML WSe_2.

■ RESULTS AND DISCUSSION

Device Fabrication. ML WSe_2 and thin h-BN are obtained by mechanical exfoliation from bulk 2H−WSe_2 (see the Supporting Information for bulk crystal growth details) and h-BN crystals (2D Semiconductors Inc.) by the polydimethylsiloxane (PDMS)-based method followed by subsequent dry transfer with the help of a micromanipulator onto the boron-doped SiO_2/Si(100) substrate (300 nm-thick SiO_2). Initially, the layer thickness is determined by the optical contrasts. This procedure has been followed to create two devices. One assembly forms the 2L-hBN/WSe_2/hBN stack (D1), while the other WSe_2/hBN stack (D2) is formed by deliberately misplacing the thin h-BN flake and the ML WSe_2 flake to yield one encapsulated area and one nonencapsulated area, followed by annealing in an Ar/H_2 atmosphere at 423 K for 3 h. Figure 1a shows the schematic of the tunnel FET device. In an effort to reduce the inhomogeneity between the devices, both the studied transistors are fabricated simultaneously on a single substrate. Si is used as a back gate to tune the carrier density in the channel. WSe_2 is confirmed to be a single layer by confocal photoluminescence (PL) measurements, as shown in Figure 1d (see the Supporting Information for details). The high quality of the encapsulated SC with thin h-BN is reflected in the high neutral exciton X° signal at low-temperature PL, as depicted in Figure 1d, compared to the defect peaks as opposed to an unencapsulated sample lying bare on the SiO_2/Si substrate, as shown in Figure S3 (see the Supporting Information), obtained from the same bulk. It is important to note that the WSe_2 beneath the thin h-BN does not come in contact with polymers during fabrication because of full encapsulation of the flake. ML WSe_2 FET devices are fabricated by patterning (methyl methacrylate)/poly(methyl methacrylate) resists using e-beam lithography. The metallic FM electrodes consisting of a superstructure formed by Co/Pt with Pt (15 Å) as the immediate contact material on top of both D1 and D2 are deposited inside an ultrahigh vacuum chamber with a base pressure of $\sim 10^{-9}$ Torr. The magnetic behavior is confirmed by the polar magneto-optical Kerr effect (see Figure S4) with the external magnetic field perpendicular to the sample surface. The channel lengths of both the devices are 4 and 3.5 μm, respectively, and the widths of the flakes are generally between 2 and 2.5 μm. The dielectric screening by h-BN on ML WSe_2 not only helps with device mobility but also protects the channel from environmental effects and degradation. The optical microscopy image shown in Figure 1b illustrates the final device geometry for single-layer WSe_2 FETs. Figure 1c illustrates the energy level diagram for ML WSe_2 with respect to the immediate contact material platinum to the channel via the thin h-BN barrier (not shown). Current−voltage ($I-V$) measurements are performed by applying a DC voltage across two electrodes and registering the current response in both devices.

DC Bias Electrical Transport and Schottky Analysis. We now examine the two-probe $I-V$ curves as a function of temperature in order to better comprehend the essence of the Schottky barrier in these devices. First, we discuss the $I-V$ characteristics for the tunnel device with Pt/h-BN contacts to ML WSe_2. Figure 2a displays $I-V$ curves on a logarithmic scale for several temperatures falling into the thermionic emission regime. The measured current response increases with the increase in temperature. The figure demonstrates a rectifying behavior from symmetric electrodes, especially at 80 K. Experimentally, even when designing symmetric electrodes, there is some difference in the widths of the electrodes in the order of "nm". In fact, it is quite difficult to make them ideally symmetric. Hence, we believe that at low temperatures, because of the slight asymmetry of the electrodes, one of the electrodes starts behaving more resistive than the other one. Therefore, the nearly symmetrical rectifying behavior in the $I_{ds}-V_{ds}$ at low temperatures is due to these back-to-back Schottky diode-like structures. A typical two-probe $I-V$ curve taken in a wide temperature range is displayed in Figure S2a (see the Supporting Information) for this device with a channel length, L, of 4 μm. Please note that our device channel length is ∼ 4 μm, while the contact widths are ∼ 1 μm. For a constant channel length, because the tunneling (Schottky barrier) changes exponentially with voltage, increasing above some voltage results in a very small change of voltage on the contacts and most of it falling on the channel, and if the channel is larger comparative to contacts, leading to a (nearly) linear IV behavior. Two-probe conductance measured at 240 K as a function of V_g is shown in Figure S2b (see the Supporting Information) and exhibits decreasing conductance as V_g is swept toward positive voltages. In fact, this characteristic behavior is seen on both devices measured throughout the wide temperature range and indicates that the devices are intrinsically p-type as fabricated. It reflects that the Fermi level

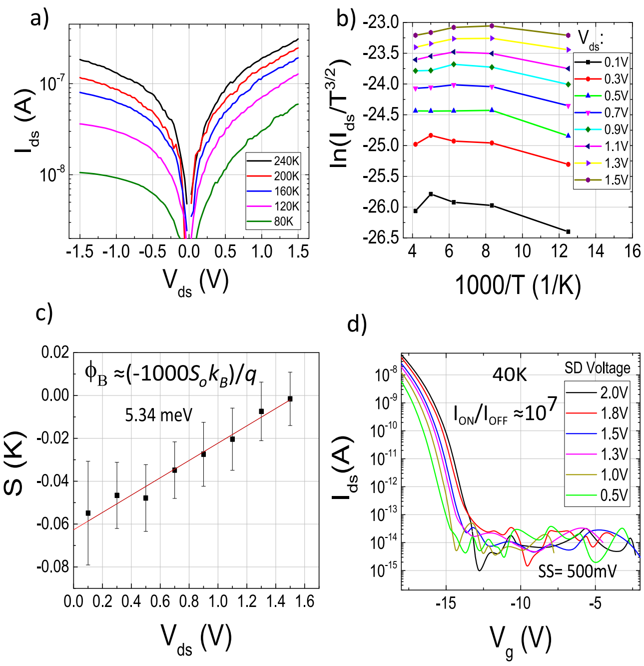

Figure 2. Charge transport in the encapsulated ML WSe_2 device at V_g = −18 V. (a) $I-V$ curves for the ML WSe_2 FET device with FM contacting WSe_2 via a tunnel barrier formed by two-layer h-BN from T = 80 to 240 K; (b) Arrhenius plot $\ln(I_{ds}/T^{3/2})$ vs $1000/T$ at different drain−source voltages V_{ds} in the thermionic emission temperature range; (c) extraction of Schottky barrier height Φ_B by taking the y-intercept value. Here, each data point represents the slope obtained from the Arrhenius plot in (b) under a specific V_{ds}; (d) current I_{ds} plotted on a logarithmic scale as extracted from a single-layer WSe_2 FET at T = 40 K and as a function of the gate voltage V_g for several values of the voltage V_{ds} between drain and source contacts. Notice that the on/off ratio approaches 10^7 and a subthreshold swing of SS ≈ 500 mV per decade.

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lies deep within the band gap close to the valence band of WSe_2, which is expected to be of a very high work function metal contact material such as platinum here. The back gate voltage V_g applied to the Si substrate results in a 500 mV subthreshold slope for every decade of current change, shown in Figure 2d, at 40 K (for 300 nm SiO_2 dielectric). Electrical transport across a Schottky contact into a semiconductor has been conventionally described by the 3D thermionic emission equation.[20]

The same format of the equation is modified into a slightly different equation when we consider devices which fall in the regime of thin 2D materials as is our case. In such a situation, the drain–source current I_{DS} can be defined by a 2D thermionic emission equation[19] instead. This equation has the form of a reduced power law where temperature dependence goes as $T^{3/2}$ for a 2D transport channel and is given by

$$I_{DS} = A^*_{2D} S T^{3/2} \exp\left[-\frac{q}{k_B T}\left(\Phi_B - \frac{V_{DS}}{n}\right)\right] \tag{1}$$

where A^* is the 2D equivalent Richardson constant, S is the contact area of the junction, q is the elementary charge, Φ_B is the Schottky barrier height, n is the ideality factor, k_B is the Boltzmann constant, and V_{DS} is the drain–source bias.

To determine Φ_B, $\ln(I_{ds}/T^{3/2})$ is plotted against $1000/T$ for various V_{DS} biases, as shown in Figure 2b. The data are linear at each bias in the thermionic emission regime, and the slope (S) is subsequently plotted in Figure 2c as a function of drain–source bias. The y-intercept of Figure 2c, denoted by S_o in the formula mentioned on the figure, yields Φ_B according to $S_o = -q\Phi_B/1000k_B$. For ML WSe_2 transistors D2 with direct Pt contacts, Φ_B is found to be ~239 meV (Figure 3b) and shows

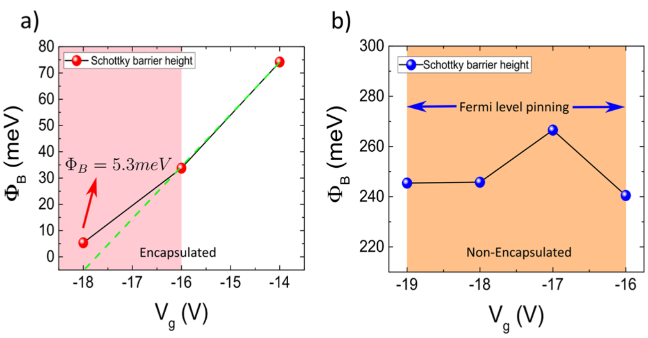

Figure 3. (a) Back-gate voltage-dependent effective Schottky barrier heights Φ_B for the two-layer hBN tunnel barrier device. The deviation from the linear response at $V_g = -16$ V (green dotted line) should define the flat band voltage (V_F) and close to the real Φ_B for Pt/hBN on ML WSe_2. The shaded pink region suggests a crossover from the thermionic regime into the pure tunneling regime. (b) Back-gate voltage-dependent effective Schottky barrier heights Φ_B for the nonencapsulated ML WSe_2 device with the direct metal/semiconductor junction. Notice the high values and nontunability of the barrier heights attributed to FLP effects (orange area).

hardly any modulation with the change of gate voltages. On the other hand, the tunnel barrier-encapsulated device D1 attains good gate tunability (Figure 3a) and shows an effective Schottky barrier height as low as 5.34 meV, as shown in Figure 2c. It is worth mentioning that the true estimate of the Schottky barrier height comes from the flat band deviation of effective Schottky values from a linear region, and because the device without encapsulation D2 does not show any signs of tunability (see Figure 3b), it is very hard to pin point the specific value of the barrier height in this case. Such an analysis, on the other hand, seemed possible with the encapsulated device, but the interference from leakage possibly via SiO_2 for a broader range of gate voltages has not enabled us to make that conclusion decisively. Even so, the lower bound for the "true" barrier height could be inferred as 32.5 meV, as shown in Figure 3a, because this value scales with the threshold gate voltage of the transistor within the temperature range where the thermionic emission model is valid. In addition, because the device can be tuned for the Schottky heights, a transition from the thermionic emission regime possibly into the tunneling dominant regime is achieved, pushing this effective value down to an ultralow value of 5.34 meV.

The D2 corresponds to direct Schottky contact by Pt to the ML WSe_2 flake. Temperature-dependent I–V characteristics show an asymmetry on either side of the bias, and the transistor behaves more like a Schottky diode, as shown in Figure S1d (see the Supporting Information). This reflects the dominance of transport assisted by thermionic emission and is consistent with the previous results[21−23] for the direct normal metal (NM)–SC junction. On the other hand, for D1, as has been shown in Figure 2a, an almost symmetric behavior in the I_{DS}–V_{DS} plot around zero bias could be seen, suggesting the dominance of tunnel transport over thermionic emission.[24] Thus, instead of increasing two-probe resistance, insertion of a 2L-hBN barrier reduces the device resistance, especially at low drain–source biases, which could be quite relevant for all practical purposes of electrical spin injection/detection performed generally at low biases.[25] The two terminal resistances at 10 K in the low bias regime exceed 500 MΩ for tunnel device D1, as shown in Figure S2 (inset). This can be confirmed quantitatively by examining the 2D Arrhenius behavior using eq 1 and extracting Φ_B. Figure 2b shows the Arrhenius plot at different drain–source bias voltages. Figure 2c displays the resulting Schottky barrier height extracted from extrapolation of slopes, as shown in Figure 2b, as 5.34 meV as discussed above. This is a dramatic decrease, of almost 98%, in Φ_B from no barrier to the 2L-hBN barrier (Figure 3a,b). Notably, a significant fact is that the barrier height, which is related to the contact resistance, can be controlled by inserting h-BN barriers. Figure 2d shows the subthreshold slope curve for the estimation of the on/off ratio for the tunnel FET. The data shown for 40 K in Figure 2d as a function of gate voltages show that the best value for this ratio is of the order of 10^7, which is comparable to previous high-performance devices made from the WSe_2 ML as the SC with the NM contacts.[26]

The Schottky barrier height is dependent solely on the work functions of the metal and SC for metals/SC junctions without interface states.[27] Research on MoS_2 Schottky contacts showed that the measured height of the Schottky barrier depends linearly on work functions.[28] However, it is an open issue whether or not interfacial states also play a part. It is known that such states can dramatically affect Φ_B through FLP,[29,30] as exhibited in our device D2. For a high density of interfacial states (DIS), Φ_B can be completely determined by the interfacial states, independent of the metal work function. The gate dependence of the barrier provides some insight into the role of interfacial states. In the conventional theory of Schottky barriers for semiconductors,[31] both work functions and interface states play a role in determining the barrier height with relative importance depending on the DIS.

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Interestingly, in the two limits of DIS = 0 (work function model) and DIS → ∞ (FLP), the Schottky barrier is independent of the electron density. However, in the intermediate regime of DIS, the Schottky barrier height decreases with increasing electron density. As the same trend is observed in our ML WSe_2 transistor D1, it provides evidence that work functions and interfacial states both play a role in determining the barrier height. Therefore, the data presented here for ML WSe_2, which also demonstrate lowering of the Schottky barrier height with the insertion of the 2L-hBN barrier, beg an explanation for the case of intermediate DIS and suggest that interfacial states are important for a full understanding of Schottky contacts to TMDCs. At the same time, the likelihood of transport being affected by intrinsic defects in the bulk and fabrication-related details could also be an open possibility. A detailed model explaining this, in addition to the experimental data and technique to probe the interface directly, is worthy of further investigation, however, out of the scope of this work.

$I-V$ measurements combined with the gate dependence provide additional insight into the impacts of h-BN barriers on Φ_B. For Pt directly in contact with ML WSe_2 without the h-BN barrier, the Schottky barrier height does not decrease considerably and varies approximately from 239 ± 5.9 to 258 ± 1.6 meV at various gate voltages, as shown in Figure 3b (blue dots). With the insertion of the 2L-hBN barrier, Φ_B varies from 5.34 ± 0.08 meV at $V_g = -18$ V to 72 ± 2.6 meV at $V_g = -14$ V. In the measured range, the direct Pt contact Schottky barrier height is never less than for Pt with 2L-hBN. A simple linear extrapolation indicates that for no barrier, Φ_B is approximately 258 meV for gate voltages of above −14 V. On the other hand, with the insertion of 2L-hBN, Φ_B is relatively low at all measured gates and goes to an ultralow value of 5.34 meV at $V_g = -18$ V. Thus, both back gate and 2L-hBN provide a wide parameter space to control the Schottky barrier height in the ML WSe_2 tunnel FET device.

■ DISCUSSION

To reconcile the case for efficient tunneling in our encapsulated device, one has to be careful to see the Arrhenius plots over a broad temperature range. To clarify this point, let us focus on the temperature dependence of conductance which serves as a fingerprint for the electronic hopping processes that are involved in the transport, as shown in the schematic in Figure 4a. In the WSe_2 system, it is reported that the selenium vacancies can introduce localized donor states inside the band gap.[32] Figure 4b shows the Arrhenius plot for T-dependent conductance at different V_{ds} at a constant gate voltage. It could be seen from temperature variation of G with different V_{ds} that the charge transport phenomena can be described by two different mechanisms, known as activation transport models, in the respective high- and low-temperature regimes, with a characteristic threshold at around $T^* = 58$ K. For this $T > T^*$, carriers with a conductivity varying like $G \approx \exp(-T_0/T)$ are dominated by the nearest-neighbor hopping mechanism. For $T < T^*$, a 2D variable-range hopping (VRH) mechanism equation with much weaker temperature dependence according to $G \approx \exp(-T_1/T)^{0.33}$ can instead be used to fit the conductance. In many low-dimensional systems, such T dependence has been observed in accordance with Mott VRH theory[33] and is a signature for transport via localized states driving the system into a strongly localized regime.[34−36] In Figure 4c, as a different set of data to verify the fitting

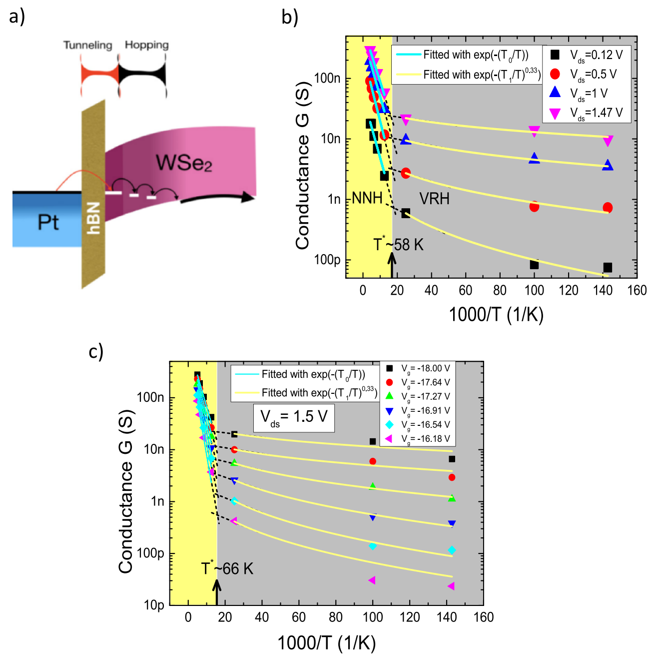

Figure 4. Evidence for hopping transport in the Pt/hBN/WSe_2 contact region; (a) band diagram for the Schottky contact region for the ML WSe_2 device. The device can be separated into three locales. The direct tunneling locale comprises the h-BN tunnel barrier and one part of Schottky contact taken together. The second locale is in the tail portion of the depletion layer where holes (electrons) transport in a hopping mannerism. The third locale is where holes (electrons) either transport in the WSe_2 channel by hopping or transport in the WSe_2 valence band (conduction band), contingent upon the carrier density. (b) Arrhenius plot of the temperature-dependent conductance G (symbols) at various V_{ds} at $V_g = -18$ V and the fitting results by the different hopping models (blue and yellow lines). Two hopping regimes are clearly separated by T^* (vertical line) corresponding to a temperature of ∼58 K. (c) Arrhenius plot of G for different values of V_g. Solid lines are fits to the data showing two distinct conduction behavior for various regions of T and V_g (charge density).

models used above, which shows temperature variation of G with different V_{gs} instead, for the same encapsulated sample D1, the slope of the Arrhenius plot changes around similar T^*, implying the same crossover of conduction mechanisms. The two temperature regions for the different hopping regimes are even more pronounced at a small drain−source bias V_{ds} of 0.12 V where the probability of contact resistance dominating the total resistance is quite high. This emphasizes that the dominant transport mechanism is hopping through the contact regions over the WSe_2 channel itself.

In this instance, we put forward an explanation that the contact region may be constituted by three different zones as depicted schematically in Figure 4a: (i) the dielectric insulating h-BN tunnel barrier, (ii) the strongly depleted zone (dark pink) underneath h-BN playing the role of an additional composite tunnel barrier, and (iii) the rear part of the depletion zone (smeared pink) of the ML WSe_2 where the hopping mechanism guarantees electronic conduction. If we pay close attention to the inhomogeneous channel composed of two components, the depletion part below h-BN and a semi-infinite section of a channel, electron hopping can profit from the electric field[37] or thermal activation energy[38] through localized states whenever there is an increase in either the bias or temperature, particularly for the VRH procedure, and can effectively reduce resistance R_{iii}. This fact could be investigated in more detail by experiments with a higher number of probes which can shed more light precisely on this subject through an elaborate investigation of channel resistances. These results are extremely promising indicators in the direction of the possibility of spin injection and transport in encapsulated ML WSe_2. Uniform h-BN barriers can provide the contact resistance needed to alleviate the conductance mismatch problem and the resistance value can be easily controlled by gate voltages, enabling the tuning of Φ_B down to almost zero, given the limits for gate leakage values (this might vary from device to device). This permits a minimization of the depletion region for a highly conductive spin transport channel.

■ CONCLUSIONS

We have examined the properties of p-type single-layer tunneling WSe_2 FET devices with FM electrodes. In particular, using 2D thermionic emission analysis by current−voltage curves, we have measured the Schottky barrier height for Pt electrodes directly in contact with WSe_2 and have attributed the nontunability to FLP effects. Remarkably, we have found that with the insertion of a thin h-BN barrier between the Pt electrode and the WSe_2 flake encapsulated by thicker h-BN, the effective Schottky barrier height can be reduced to an ultralow one by as much as 97.7%. We have shown that the barrier height can be manipulated by both the h-BN presence and back gate voltages. From systematic studies of the bias, temperature, and back-gate voltage dependence of Schottky barrier heights, we surmise that in order to maintain a balance between interface tunneling resistance and channel resistance, which is mandatory for the observation of two-terminal spin signals, the understanding and the behavior of hopping via localized states in the contact depletion region could play a central role. Elimination of metal/TMDC chemical interactions by the h-BN insertion layer along with full boron nitride encapsulation of the channel allows us to better preserve the intrinsic properties of the 2D channel. The discussion presented here for hopping via h-BN tunnel barriers to 2D semiconductors allows us to satisfactorily describe and reproduce their experimental electrical response within the Schottky−Mott limit. Such low barrier heights and the ability to optimize them encourage and open up the avenues for future studies on purely electrical spin transport in MLs of WSe_2. These results promise to be important not only to those interested in WSe_2 in particular but also to the larger community exploiting 2D materials for optoelectronic and spintronics applications.

■ METHODS

ML WSe_2 and thin h-BN are obtained by mechanical exfoliation from bulk 2H−WSe_2 grown by chemical vapor transport (see the Supporting Information for bulk crystal growth details) and h-BN crystals (2D Semiconductors Inc.) by the PDMS-based method followed by subsequent dry transfer with the help of a micro-manipulator onto the boron-doped SiO_2/Si(100) substrate (300 nm-thick SiO_2). Initially, the layer thickness is determined by the optical contrasts. Room temperature PL spectra were acquired with a home-built laser scanning confocal spectromicroscope with 532 nm laser excitation. The low-temperature PL spectra of WSe_2 MLs were measured by a micro-PL setup. The setup consist of a three-axis positioner and a 100× objective lens (NA = 0.82) integrated in a cryogen-free cryostat with a base temperature of 4.2 K. A He−Ne laser with a wavelength of 632.8 nm was used to excite the WSe_2. The charge transport measurements have been performed in a four-probe cryostat system by *Lakeshore* by varying temperature from 6.6 to 280 K with a base pressure of 2×10^{-6} mbar. For the back-gated two-terminal measurements, as described in Figure 2, we have used one of the Keithley 2636B channels to apply the drain−source bias V_{ds} and measure drain−source current I_{ds} and used the other Keithley 2636B channel to apply the back-gate voltage V_g. Estimation of the mobility of our FET device with the 2L h-BN tunnel junction has been performed by the $I_{DS} - V_G$ characterization. All measurements reported here use a voltage-biased scheme.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.0c01025.

Details of bulk single-crystal preparation, room temperature and low-temperature PL measurements, details of electrical measurements, polar MOKE measurement of the Co/Pt-layered FM superstructure at room temperature, and optical images of the device constituents (PDF)

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■ REFERENCES

(1) Lin, Y.-F.; Xu, Y.; Wang, S.-T.; Li, S.-L.; Yamamoto, M.; Aparecido-Ferreira, A.; Li, W.; Sun, H.; Nakaharai, S.; Jian, W.-B.; Ueno, K.; Tsukagoshi, K. Ambipolar $MoTe_2$ Transistors and Their Applications in Logic Circuits. *Adv. Mater.* **2014**, *26*, 3263−3269.

(2) Pradhan, N. R.; Rhodes, D.; Feng, S.; Xin, Y.; Memaran, S.; Moon, B.-H.; Terrones, H.; Terrones, M.; Balicas, L. Field-Effect Transistors Based on Few-Layered α-MoTe 2. *ACS Nano* **2014**, *8*, 5911−5920.

(3) Li, H.; Yin, Z.; He, Q.; Li, H.; Huang, X.; Lu, G.; Fam, D. W. H.; Tok, A. I. Y.; Zhang, Q.; Zhang, H. Fabrication of Single- and Multilayer MoS2 Film-Based Field-Effect Transistors for Sensing NO at Room Temperature. *Small* **2012**, *8*, 63−67.

(4) Withers, F.; Del Pozo-Zamudio, O.; Mishchenko, A.; Rooney, A. P.; Gholinia, A.; Watanabe, K.; Taniguchi, T.; Haigh, S. J.; Geim, A. K.; Tartakovskii, A. I.; Novoselov, K. S. Light-Emitting Diodes by Band-Structure Engineering in Van der Waals Heterostructures. *Nat. Mater.* **2015**, *14*, 301−306.

(5) He, Q.; Zeng, Z.; Yin, Z.; Li, H.; Wu, S.; Huang, X.; Zhang, H. Fabrication of Flexible MoS2 Thin-Film Transistor Arrays for Practical Gas-Sensing Applications. *Small* **2012**, *8*, 2994−2999.

(6) Wang, X.; Wang, P.; Wang, J.; Hu, W.; Zhou, X.; Guo, N.; Huang, H.; Sun, S.; Shen, H.; Lin, T.; Tang, M.; Liao, L.; Jiang, A.; Sun, J.; Meng, X.; Chen, X.; Lu, W.; Chu, J. Ultrasensitive and Broadband MoS2 Photodetector Driven by Ferroelectrics. *Adv. Mater.* **2015**, *27*, 6575−6581.

(7) Nguyen, D. A.; Oh, H. M.; Duong, N. T.; Bang, S.; Yoon, S. J.; Jeong, M. S. Highly Enhanced Photoresponsivity of a Monolayer WSe2 Photodetector with Nitrogen-Doped Graphene Quantum Dots. *ACS Appl. Mater. Interfaces* **2018**, *10*, 10322−10329.

(8) Radisavljevic, B.; Kis, A. Mobility Engineering and a Metal-Insulator Transition in Monolayer MoS2. *Nat. Mater.* **2013**, *12*, 815−820.

(9) Radisavljevic, B.; Radenovic, A.; Brivio, J.; Giacometti, V.; Kis, A. Single-layer MoS2 Transistors. *Nat. Nanotechnol.* **2011**, *6*, 147−150.

(10) Schwierz, F. Graphene Transistors. *Nat. Nanotechnol.* **2010**, *5*, 487−496.

(11) Xiao, D.; Liu, G.-B.; Feng, W.; Xu, X.; Yao, W. Coupled Spin and Valley Physics in Monolayers of MoS2 and Other Group-VI Dichalcogenides. *Phys. Rev. Lett.* **2012**, *108*, 196802.

(12) Chen, X.; Yan, T.; Zhu, B.; Yang, S.; Cui, X. Optical Control of Spin Polarization in Monolayer Transition Metal Dichalcogenides. *ACS Nano* **2017**, *11*, 1581−1587.

(13) Mott, N. F. Note on the Contact Between a Metal and an insulator or Semiconductor. *Math. Proc. Cambridge Philos. Soc.* **1938**, *34*, 568−572.

(14) Ghiasi, T. S.; Quereda, J.; van Wees, B. J. Bilayer h-BN Barriers for Tunneling Contacts in Fully-Encapsulated Monolayer MoSe2 Field-Effect Transistors. *2D Mater.* **2018**, *6*, 015002.

(15) Cui, X.; et al. Low-Temperature Ohmic Contact to Monolayer MoS2 by Van der Waals Bonded Co/h-BN Electrodes. *Nano Lett.* **2017**, *17*, 4781−4786.

(16) Chen, J.-R.; Odenthal, P. M.; Swartz, A. G.; Floyd, G. C.; Wen, H.; Luo, K. Y.; Kawakami, R. K. Control of Schottky Barriers in Single Layer MoS2 Transistors with Ferromagnetic Contacts. *Nano Lett.* **2013**, *13*, 3106−3110.

(17) Allain, A.; Kang, J.; Banerjee, K.; Kis, A. Electrical Contacts to Two-Dimensional Semiconductors. *Nat. Mater.* **2015**, *14*, 1195−1205.

(18) Zhou, B. T.; Taguchi, K.; Kawaguchi, Y.; Tanaka, Y.; Law, K. Spin-Orbit Coupling Induced Valley Hall Effects in Transition-Metal Dichalcogenides. *Commun. Phys.* **2019**, *2*, 26.

(19) Anwar, A.; Nabet, B.; Culp, J.; Castro, F. Effects of Electron Confinement on Thermionic Emission Current in a Modulation Doped Heterostructure. *J. Appl. Phys.* **1999**, *85*, 2663−2666.

(20) Bhuiyan, A. S.; Martinez, A.; Esteve, D. A New Richardson Plot for Non-Ideal Schottky Diodes. *Thin Solid Films* **1988**, *161*, 93−100.

(21) Jariwala, D.; Sangwan, V. K.; Late, D. J.; Johns, J. E.; Dravid, V. P.; Marks, T. J.; Lauhon, L. J.; Hersam, M. C. Band-like Transport in High Mobility Unencapsulated Single-Layer MoS2 Transistors. *Appl. Phys. Lett.* **2013**, *102*, 173107.

(22) Yamaguchi, T.; Moriya, R.; Inoue, Y.; Morikawa, S.; Masubuchi, S.; Watanabe, K.; Taniguchi, T.; Machida, T. Tunneling Transport in a Few Monolayer-Thick WS2/Graphene Heterojunction. *Appl. Phys. Lett.* **2014**, *105*, 223109.

(23) Moriya, R.; Yamaguchi, T.; Inoue, Y.; Morikawa, S.; Sata, Y.; Masubuchi, S.; Machida, T. Large Current Modulation in Exfoliated-Graphene/MoS2/Metal Vertical Heterostructures. *Appl. Phys. Lett.* **2014**, *105*, 083119.

(24) Omar, S.; van Wees, B. J. Graphene-WS2 Heterostructures for Tunable Spin Injection and Spin transport. *Phys. Rev. B* **2017**, *95*, 081404.

(25) Liang, S.; Yang, H.; Renucci, P.; Tao, B.; Laczkowski, P.; Mc-Murtry, S.; Wang, G.; Marie, X.; George, J.-M.; Petit-Watelot, S.; et al. Electrical Spin Injection and Detection in Molybdenum Disulfide Multilayer Channel. *Nat. Commun.* **2017**, *8*, 14947.

(26) Liu, W.; Cao, W.; Kang, J.; Banerjee, K. High-Performance Field-Effect-Transistors on Monolayer-WSe2. *ECS Trans.* **2013**, *58*, 281−285.

(27) Neamen, D. J. *Semiconductor Physics and Devices*; McGraw-Hill Education: Europe, 2012; pp 336−337.

(28) Das, S.; Chen, H.-Y.; Penumatcha, A. V.; Appenzeller, J. High Performance Multilayer MoS2 Transistors with Scandium Contacts. *Nano Lett.* **2012**, *13*, 100−105.

(29) Hughes, G. J.; McKinley, A.; Williams, R. H.; McGovern, I. T. Metal-Gallium Selenide Interfaces-Observation of the True Schottky Limit. *J. Phys. C: Solid State Phys.* **1982**, *15*, L159−L164.

(30) LaGasse, S. W.; Dhakras, P.; Watanabe, K.; Taniguchi, T.; Lee, J. U. 467 Gate-Tunable Graphene-WSe2 Heterojunctions at the Schottky-Mott Limit. *Adv. Mater.* **2019**, *31*, 1901392.

(31) Cowley, A. M.; Sze, S. M. Surface States and Barrier Height of Metal-Semiconductor Systems. *J. Appl. Phys.* **1965**, *36*, 3212−3220.

(32) Stanford, M. G.; Pudasaini, P. R.; Gallmeier, E. T.; Cross, N.; Liang, L.; Oyedele, A.; Duscher, G.; Mahjouri-Samani, M.; Wang, K.; Xiao, K.; Geohegan, D. B.; Belianinov, A.; Sumpter, B. G.; Rack, P. D. High Conduction Hopping Behavior Induced in Transition Metal Dichalcogenides by Percolating Defect Networks: Toward Atomically Thin Circuits. *Adv. Funct. Mater.* **2017**, *27*, 1702829.

(33) Hamilton, E. M. Variable Range Hopping in a Non-Uniform Density of States. *Philos. Mag. A* **1972**, *26*, 1043−1045.

(34) Qiu, H.; Xu, T.; Wang, Z.; Ren, W.; Nan, H.; Ni, Z.; Chen, Q.; Yuan, S.; Miao, F.; Song, F.; Long, G.; Shi, Y.; Sun, L.; Wang, J.; Wang, X. Hopping Transport Through Defect-Induced Localized States in Molybdenum Disulphide. *Nat. Commun.* **2013**, *4*, 2642.

(35) Han, M. Y.; Brant, J. C.; Kim, P. Electron Transport in Disordered Graphene Nanoribbons. *Phys. Rev. Lett.* **2010**, *104*, 056801.

(36) Yu, Z.; Song, X. Variable Range Hopping and Electrical Conductivity along the DNA Double Helix. *Phys. Rev. Lett.* **2001**, *86*, 6018−6021.

(37) Lu, Y.; Lacour, D.; Lengaigne, G.; Le Gall, S.; Suire, S.; Montaigne, F.; Hehn, M.; Wu, M. W. Electrical Control of Interfacial Trapping for Magnetic Tunnel Transistor on Silicon. *Appl. Phys. Lett.* **2014**, *104*, 042408.

(38) Lu, Y.; Tran, M.; Jaffrès, H.; Seneor, P.; Deranlot, C.; Petroff, F.; George, J.-M.; Lépine, B.; Ababou, S.; Jézéquel, G. Spin-Polarized Inelastic Tunneling through Insulating Barriers. *Phys. Rev. Lett.* **2009**, *102*, 176801.

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