Ultimate Scaling of CMOS Logic Devices with Ge and III-V Materials

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ON THE COVER: Ultimate Scaling of CMOS Logic Devices with Ge and III–V Materials. This issue of MRS Bulletin presents an overview of the major successes and remaining critical issues in the materials research on high-mobility channel materials for advanced complementary metal oxide semiconductor (CMOS) devices. The availability of III–V materials on Si opens up new opportunities for integrating new functionalities on silicon, providing a driving force for this research area. The cover shows a density functional theory molecular dynamics model of the amorphous Al2O3/Ge(100) interface after 700 K annealing. Green—Ge; blue—Al; red—O; and white—H. In this model, the oxide/semiconductor interface has subnanometer scale atomic migration and lattice distortion, creating dangling bonds that induce defect states and demonstrating the need for molecular interface passivation for optimal device performance. Image courtesy of E.A. Chagarov and A.C. Kummel. The inset is a cross-sectional high-resolution transmission electron microscopy image of a 4.5-nm Al2O3/Ge2O3(Gd2O3)/InGaAs sample rapid thermal annealed to 800°C for 10 s in a N2 ambient. Image courtesy of Y.J. Lee and L.T. Tung.

ALSO IN THIS ISSUE: On the Genesis of Nuclei and Phase Separation on an Atomic Scale. Shown on the cover is the effects of vacancy-solute binding energies on the growth and coarsening of precipitates. Green—N; blue—Cr; and red—Al. See Figure 4 on p. 540 for more information.

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