Effective reduction of interfacial traps in Al$_2$O$_3$/GaAs (001) gate stacks using surface engineering and thermal annealing


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To effectively passivate the technologically important GaAs (001) surfaces, in situ deposition of Al$_2$O$_3$ was carried out with molecular beam epitaxy. The impacts of initial GaAs surface reconstruction and post-deposition annealing have been systematically investigated. The corresponding interfacial state density ($D_{it}$) were derived by applying the conductance method at 25 and 150 °C on both p-type and n-type GaAs metal-oxide-semiconductor capacitors to establish the $D_{it}$ spectra in proximity of the critical midgap region. We show that significant reduction of $D_{it}$ near the midgap is achieved by applying an optimized thermal annealing on samples grown on a Ga-rich (4 × 6) reconstructed surface. © 2010 American Institute of Physics. [doi:10.1063/1.3488813]

The quest for technologies beyond the 15 nm node complementary metal-oxide-semiconductor (CMOS) devices has now called for research of high κ dielectrics on alternative channel materials such as Ge and III-V compound semiconductors with inherently higher carrier mobility than those of Si. Among the III-V’s and the related MOS devices, GaAs nMOS has received intensive efforts in the past decades, owing to GaAs’s superior bulk electron mobility (8500 cm$^2$/V s) and its lattice parameter (5.65 Å) nearly identical to that of Ge. Direct oxidation of GaAs surfaces using thermal, anodic, and plasma methods have failed to produce an insulator-GaAs heterointerface with a meaningful measure of interfacial state density ($D_{it}$).\(^1\)

Reducing the high $D_{it}$'s on oxide/GaAs, particularly those near the GaAs midgap region, is an important issue for realizing GaAs MOS field-effect-transistors (MOSFETs) with surface inversion.\(^3,4\) The oxide/GaAs interface with low $D_{it}$ was not achieved until the discovery of direct deposition of high κ oxides such as Ga$_2$O$_3$(Ga$_2$O$_3$) [GGO] and Ga$_2$O$_3$ on GaAs in the 1990s.\(^5,6\) However, unlike GGO, most other high-κ dielectrics on GaAs exhibit high $D_{it}$ values at the GaAs midgap region,\(^7\) resulting in serious Fermi-level pinning, and thus preventing a proper inversion response required for the inversion-channel GaAs MOS devices. Sulfur passivation\(^8-10\) and/or insertion of interfacial passivation layer of Si or Ge (Refs. 11–13) on GaAs may have decreased $D_{it}$ values in regions away from the midgap, but fail to effectively reduce the high midgap $D_{it}$ peak.

Moreover, the initial GaAs surface reconstructions for GaAs MOS devices have also been investigated, and shown to have limited success.\(^14-17\) Among them, the dielectric/GaAs interfaces started with a variety of GaAs surface reconstructions have been studied by x-ray photoelectron spectroscopy (XPS) and photoluminescence (PL).\(^15-17\) However, there are few reports to correlate electrical properties and their corresponding $D_{it}$ spectra of GaAs MOS devices with surface reconstruction of the starting GaAs substrate, prior to high κ oxide deposition. Furthermore, most of the electrical characteristics were studied using conventional capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics measured at room temperatures. Due to a larger energy band gap of GaAs compared to that of Si, interfacial traps of the dielectric/GaAs interfaces near the midgap are too slow to respond to the usual C-V and G-V characterization frequencies (100 Hz–1 MHz) at room temperatures; consequently, only a small portion of $D_{it}$ spectrum away from the midgap region has been measured.\(^18\)

In this work, this inadequacy is remedied by performing additional C-V and G-V measurements at a high temperature of 150 °C to probe $D_{it}$ spectrums around the midgap region. The $D_{it}$ distribution as a function of the energy above valence-band maximum ($E_v$) has been derived by C-V and G-V measurements at 25 and 150 °C on both n-type and p-type GaAs MOS capacitors (MOSCAPs) with the gate dielectric Al$_2$O$_3$ deposited using molecular beam epitaxy (MBE). Furthermore, the influence on the $D_{it}$ of the Al$_2$O$_3$/GaAs interfaces with the GaAs initial surface reconstructions and the systematic postannealing conditions is reported. We found that post annealing at 550 °C for 60 min and 650 °C for 30 s on samples grown on a Ga-rich (4 × 6) reconstructed surface have led to significant reduction of $D_{it}$ near the midgap.

The growth of GaAs epilayers was carried out in a 200 mm Riber III-V MBE chamber. Reflection high-energy electron diffraction (RHEED) was used to monitor the growth, and to examine the GaAs surface reconstructions prior to the oxide growth. Three different surface reconstructions of GaAs (001) were studied: the As-rich (2 × 4) surface, the As-covered (100%) c(4 × 4) surface, and the Ga-rich (4 × 6) surface. Here we report only the latter two
reconstructed surfaces, which correspond to the highest arsenic and gallium surface coverage, respectively. The 0.3 \( \mu \text{m} \) thick GaAs buffer layers were grown at 580 °C under As-rich conditions with \( \text{P(As)} = 1.8 \times 10^{-5} \) Torr. The substrate temperature was cooled down below 350 °C under As overpressure, leading to a \((4 \times 4)\) reconstructed, As-covered surface. The samples were subsequently \textit{in situ} transferred to an oxide molecular beam deposition chamber and heated up in UHV to 580 °C for 5 min to form the Ga-rich \((4 \times 6)\) surface reconstruction. \( \text{Al}_2\text{O}_3 \) films 9 nm thick were deposited by evaporating aluminum from an effusion cell under an atomic oxygen flux of \( \text{P(O)} \sim 3 \times 10^{-6} \) Torr using a plasma source. During the oxide deposition, the substrate temperature was kept \( \sim 250 \) °C. The samples were postannealed to optimize the oxide and interface quality under nitrogen ambient at various temperatures and dwelling durations. After the annealing, Ni metal gate was deposited through a shadow mask. Ohmic contacts to the back side of the substrates of the \( \text{p}-\) and \( \text{n}-\) type GaAs were made through the deposition of AuZn/Au and AuGe/NiAu multi-layers, respectively. C-V and G-V characteristics of these MOSCAPs were measured by using Agilent 4284 A. The corresponding \( D_{\text{i}} \)'s of these MOSCAPs were calculated by the conductance method.\(^\text{19}\)

C-V characteristics of \( \text{Al}_2\text{O}_3/p\)-type GaAs MOSCAPs (with a Ga-rich surface reconstruction) annealed under various conditions have been summarized in Fig. 1: (a) annealing at 550 °C for 20 min, (b) at 550 °C for 60 min, (c) 550 °C for 60 min followed by 650 °C for 30 s, (d) 550 °C for 60 min followed by 650 °C for 20 min, and (e) 550 °C for 60 min followed by 750 °C for 30 s. All the C-V curves denoted as (I) were measured at 25 °C, and are well behaved with almost identical characteristics for various annealing conditions. This is because only a small range of interfacial traps with energies of 0.3–0.5 eV lying above the valence band edge (\( E_v \)) (Ref. 18) in these samples was probed at 25 °C and the measured \( D_{\text{i}} \)'s are nearly the same of \( \sim 10^{12} \) eV\(^{-1}\) cm\(^{-2}\) in this narrow region. In contrast, C-V measurements denoted as (II) were performed at 150 °C, probing the interfacial traps covering the midgap region. Pronounced trap-induced capacitance responses, manifested as the “hump” located in the depletion region, were observed at low frequencies, consistent with those reported previously.\(^\text{8,12,17}\)

As shown in Fig. 1(II), annealing condition (b) and (c) show much smaller humps than those of (a), (d), and (e), indicating an improved interfacial quality. These results reveal that the long-time annealing at a medium temperature of 550 °C helps to reduce the hump [Figs. 1(a) and 1(b)], and the annealing at 550 °C for 60 min followed by 650 °C for 30 s [Fig. 1(c)] is the optimized annealing condition responsible for the lowest values of \( D_{\text{i}} \) [Fig. 3(a)] and the smallest frequency dispersion in depletion. The heat treatments of a prolonged duration at 650 °C and/or at higher annealing temperature, such as 650 °C for 20 min [Fig. 1(d)] or

**FIG. 1.** (Color online) C-V measurements on Ni/\( \text{Al}_2\text{O}_3(9 \text{ nm})/p\)-type GaAs MOSCAPs with Ga-rich GaAs reconstructed surface: (i) C-V curves measured at 25 °C, and (ii) C-V curves measured at 150 °C.

**FIG. 2.** (Color online) C-V curves of GaAs MOSCAPs started with Ga-rich surface on (a) \( p\)-type and (b) \( n\)-type substrates, and started with As-covered surface on (c) \( p\)-type and (d) \( n\)-type substrates.
750 °C [Fig. 1(e)], tend to deteriorate the interfacial quality. Recent XPS study on the Al2O3/GaAs interface revealed the interdiffusion of Ga into Al2O3 at elevated temperatures over 750 °C. Nevertheless, all the Al2O3/GaAs MOSCAPs demonstrated low gate leakage current densities at V_fb-1 V under various annealing conditions (not shown here), which are lower than 10^{-7} A/cm² and 10^{-6} A/cm², measured at 25 °C and 150 °C, respectively, suggesting that the good insulating property of Al2O3 is still maintained.

Figure 2 shows the C-V characteristics of MOSCAPs of Ga-rich and As-covered samples of both p-type and n-type, treated with the optimized annealing condition described above. As expected, all the corresponding C-V results at 25 °C show negligible differences. The C-V and G-V taken at 25 °C fail to detect notable D_ it at midgap region near the critical midgap region. The low D_ it at midgap region indicates the optimized GaAs MOS structures will show proper inversion response, which may lead to high-performance inversion-channel GaAs MOSFETs.

In summary, a significant reduction of the midgap peak in D_ it has been demonstrated for the first time in Al2O3/GaAs MOSCAPs by employing in situ MBE oxide growth on a Ga-rich (4×4) reconstructed GaAs (001) surface as opposed to the As-covered (4×4) reconstructed surface, followed by an optimized thermal annealing at 550 °C for 60 min and 650 °C for 30 s. Furthermore, C-V and G-V measurements conducted at elevated temperatures at 150 °C provided the essential assessment of the interfacial quality near the critical midgap region. The low D_ it at midgap region indicates the optimized GaAs MOS structures will show proper inversion response, which may lead to high-performance inversion-channel GaAs MOSFETs.

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