Depletion-mode In$_{0.2}$Ga$_{0.8}$As/GaAs MOSFET with molecular beam epitaxy grown Al$_2$O$_3$/Ga$_2$O$_3$(Gd$_2$O$_3$) as gate dielectrics

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Depletion-mode In$_{0.2}$Ga$_{0.8}$As/GaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) were fabricated with molecular beam epitaxy (MBE) grown Al$_2$O$_3$/Ga$_2$O$_3$(Gd$_2$O$_3$) as the gate dielectric in two comparable processes. In the “metal-gate-last” process, a 12 µm gate-length depletion-mode n-channel InGaAs/GaAs MOSFET with a Gd$_2$O$_3$(Ga$_2$O$_3$) gate oxide 6 nm thick shows an accumulated drain current density of 135 mA/mm at $V_{gs}$=2 V. In the other process of “metal-gate-first” process, the device with same gate dielectric, channel, and gate length exhibits a larger drain current density of 175 mA/mm at the same gate bias. In addition, there is a broader transfer characteristics and higher extrinsic peak transconductance of 48 mS/mm in the metal-gate-first process. MOS capacitors from both processes have exhibited excellent capacitance–voltage (C–V) characteristics with minor dispersion, negligible hysteresis, and $k$ values of 13.7–13.9 in Ga$_2$O$_3$(Gd$_2$O$_3$).

1. Introduction

The Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) are approaching the ultimate scaling limit in the high-speed applications. With high-electron mobility and rich band gap engineering, III–V compound semiconductors, such as InGaAs, are now being considered as strong contenders for alternative channel materials for complementary MOS (CMOS) technologies beyond the 22–16 nm node.

Two approaches, molecular beam epitaxy (MBE) grown Ga2O3(Gd2O3) [GGO] [1,2] and Gd 2O3 [3], and atomic layer deposited (ALD) Al 2O3 [4–6] and HfO 2 [7,8], have achieved low oxides in those cases using MBE-GGO [10,16]. GGO, containing rare earth Gd, tends to absorb moisture during air exposure, thus degrading the electrical properties [17]. In-situ deposited Al2O3 was found to be very effective in protecting GGO from absorbing moisture to give an excellent thermodynamic stability [18,19]. In this work, in-situ MBE-Al2O3/GGO was employed as a gate dielectric in fabricating D-mode In$_{0.2}$Ga$_{0.8}$As MOSFET using two processes: “metal-gate-last” (denoted by process A) and “metal-gate-first” (denoted by process B).

2. Oxide growth, device fabrication, and characterization

The device wafers were grown in a multi-chamber MBE/analysis system [1]. A Si-doped In$_{0.2}$Ga$_{0.8}$As (7 nm)/GaAs (90 nm) channel with a doping concentration of $4 \times 10^{17}$ cm$^{-2}$ was grown on semi-insulating GaAs (1 0 0) substrate. The wafers with freshly grown InGaAs/GaAs epi-layers were then moved to the oxide chambers for Al2O3/GGO growth [18,19]. A GGO dielectric 6 nm thick was MBE-deposited on InGaAs/GaAs channels at a substrate temperature 520 °C. An in-situ Al2O3 capping layer 2 nm thick was then deposited on GGO.

D-mode devices are fabricated in a ring-gate pattern. Device isolations (such as ion implantations) are not needed in the ring-gate approach. As a consequence, it is easier to fabricate such devices. The detailed process steps are listed in Table 1: in process A, the ohmic metal was first formed by oxide wet etching, Pd/Ge/Ti/Pt (300/600/300/300 Å) ohmic metal deposition/lift-off, and followed by ohmic-contact alloying in N$_2$ ambience at 400 °C for 10 s. The gate metal, Ti/Au, was subsequently formed by a lift-off
process. In process B, the gate metal, TiN, was firstly deposited on gate dielectrics by RF-sputtering. Subsequently, the gate pattern was formed with inductively coupled plasma reactive ion etching (ICP-RIE) and then the ohmic metal was formed with a process similar to that in process A.

On the same wafers as the D-mode MOSFETs, MOSCAPs were fabricated for characterizing the MOS structures. Therefore, the MOSCAPs underwent the same processes A and B as the MOSFETs, including all the chemical and thermal treatments. The electrical characteristics of the MOSCAPs and MOSFETs were measured using Agilent 4156C and 4284.

### 3. Device characteristics and discussion

Excellent capacitance–voltage (C–V) characteristics with minor dispersion (~6%), as shown in Fig. 1, were measured from the MOSCAPs. The dielectric constants of GGO are calculated to be 13.7 and 13.9 (at 1 MHz) for MOSCAPs fabricated with processes A and B, respectively (with that of Al₂O₃ assumed to be 8). The flatband voltages \( V_{FB} \) are calculated to be 0.48 and 0.54 V for the MOSCAPs with process A and B, respectively. The higher flatband voltage in the B-processed MOSCAP is partly due to a larger work function of TiN (4.8 eV) gate than that of Ti (4.3 eV)/Au gate used in the A-processed MOSCAP. Note that the major portion of \( V_{FB} \) is caused by the work function difference between the gate metal and In₀.₂Ga₀.₈As. Some part of it may come from the different amount of oxide traps, resulted from the two different processes.

The differences between the measured and theoretical C–V curve (\( \Delta V_{FB} \), flatband voltage shift) indicate that there are relatively lower oxide traps for the B-processed MOSCAP, as shown in the insets in Fig. 1(a) and (b). Besides, the slightly stretched C–V curve measured from the A-processed MOSCAP indicates a relatively higher surface roughness, which affects the electrical performance. Note that the theoretical C–V curve was obtained assuming an interfacial density of state to be 0, and considering the work functions of gate metal and In₀.₂Ga₀.₈As. Well-behaved C–V curves of both MOSCAPs demonstrate the robustness of the \( \text{Al}_₂\text{O}_₃|\text{Ga}_₂\text{O}_₃|\text{Gd}_₂\text{O}_₃|\text{In}_₀.₂\text{Ga}_₀.₈\text{As} \) hetero-structure, which has withstood severe thermal and chemical treatments during the device fabrication.

D-mode In₀.₂Ga₀.₈As/GaAs MOSFETs with a 12 μm gate-length and a nanometer thick \( \text{Al}_₂\text{O}_₃|\text{Ga}_₂\text{O}_₃|\text{Gd}_₂\text{O}_₃ \) dual-layer dielectric have demonstrated excellent performances with both process A and B (Figs. 2 and 3). The drain current–voltage \( (I_d–V_d) \) curve in Fig. 2 exhibits a high saturation drain current \( (I_{d,sat}) \) of 135 mA/mm (at \( V_g=2 V \) and \( V_d=5 V \)) with process A and a higher one of 175 mA/mm (at \( V_g=2 V \) and \( V_d=5 V \)) with process B. The data reveal that the Al₂O₃ capping layer has effectively protected GGO in both processing approaches. Moreover, better device performances exhibited by D-mode MOSFET fabricated with process B may be due to a better interface between the gate dielectric and the channel. This may be attributed to the fact that the gate dielectric/In₀.₂Ga₀.₈As interface in process B has been kept away from chemicals/water during the processing steps.

When normalized to a gate length of 0.8 μm with the consideration of both the source- and drain-gate distances, the maximum drain current density is ~460 mA/mm for the device that underwent process B. The performance is comparable to that of a conventional D-mode device configuration reported by Wang et al. [20] in a GaAs MOSFET with GGO gate dielectric 38 nm thick, Tsai et al. [9] in an In₀.₂Ga₀.₈As MOSFET with GGO 54 nm thick, and Ye et al. [4] in an In₀.₂Ga₀.₈As MOSFET with ALD-Al₂O₃ 16 nm thick. Our data, however, compare very favorably with those of ring-gate D-mode MOSFETs with PVD HfO₂ gate dielectrics and Si and Ge as interfacial layers [21,22]. Note that in the
D-mode devices, drain currents are not simply linearly scaled with gate length. The S-G and D-G distances have to be taken into consideration. Therefore, the extrapolation of drain current with gate length reported in Refs. [21,22] is inadequate.

A similar phenomenon is also observed from the transfer characteristics in Fig. 3. The device undergoing process B exhibits a maximum extrinsic transconductance of 48 mS/mm, which is higher than 38 mS/mm obtained from the device undergoing processes A. For process B, a better interface between the gate dielectric and the channel is implied, and the extrinsic transconductance of 130 mS/mm (if normalized to 0.8 μm gate length with the consideration of the S-G and D-G distances) is also comparable with other works.

4. Conclusion

D-mode In_{0.2}Ga_{0.8}As/GaAs MOSFETs in a ring-gate pattern using Al_{2}O_{3}/GGO as the gate dielectrics were successfully fabricated. The high saturation drain currents and the broad transfer characteristics in transconductance indicate a high-quality interface between nanothick Ga_{2}O_{3}(Gd_{2}O_{3}) and the In_{0.2}Ga_{0.8}As/GaAs n-channels, resulting from the protection of the in-situ deposited Al_{2}O_{3}. A better device performance from the “metal-gate-first” processed D-mode MOSFET may be possible due to an even better interface between gate dielectric and semiconductor channel because of the extra protection from the gate metal deposited at the very beginning.

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References
