Defining new frontiers in electronic devices with high \( \kappa \) dielectrics and interfacial engineering

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Abstract

\( \text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3) \), a high \( \kappa \) gate dielectric, ultrahigh vacuum (UHV)-deposited on GaAs and InGaAs has unpinned the Fermi level in the high-electron-mobility III–V compound semiconductors for the first time. Systematic heat treatments under various gases and temperatures were studied to achieve low leakage currents of \( 10^{-8}–10^{-9} \) A/cm\(^2\) and low interfacial density of states (\( D_{it} \)) in the range of \( <10^{11} \) cm\(^{-2}\) eV\(^{-1}\). By removing moisture from the oxide, thermodynamic stability of the \( \text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)/\text{GaAs} \) heterostructures and the interfaces were achieved with high temperature annealing, the oxide remains amorphous and the interface remains intact with atomic smoothness and sharpness. The Fermi-level unpinning in atomic layer deposition (ALD) \( \text{Al}_2\text{O}_3 \) ex-situ deposited on InGaAs was achieved. Recent work of extremely high-quality nano-thick single crystal oxides of \( \gamma \)-\( \text{Al}_2\text{O}_3 \) and bixbyite cubic \( \text{Sc}_2\text{O}_3 \) epitaxially grown on Si (111) is discussed. Interfacial manipulation is essential in giving excellent results presented in the paper. X-ray diffraction, reflectivity, and X-ray photoelectron spectroscopy using synchrotron radiation are critical in probing the interfacial properties.

Keywords: B1 oxides; B1 high \( \kappa \) gate dielectrics; B2 semiconducting III–V materials; B3 \( D_{it} \); A1 X-ray diffraction; A1 X-ray photoelectron spectroscopy

1. Introduction

Interfaces between oxides and semiconductors always play a critical role in determining the electronic and electrical properties of the heterostructures. Often the interfaces determine the crystallographic and transport properties of the grown (or the deposited) oxides. The perfection in the well known \( \text{SiO}_2-\text{Si} \) interface enables the design and large-scale applications of complementary metal-oxide-semiconductor (CMOS) transistors and integrated circuits. The aggressive scaling of Si CMOS device has called for alternative high \( \kappa \) gate dielectrics replacing conventional \( \text{SiO}_2 \) (\( \kappa =3.9 \)). Intense research on this area over the last several years has identified a number of binary oxides and silicates with impressive dielectric properties [1]. However, high Coulomb scattering from charge trapping and the phonon issue related to the high \( \kappa \) gate dielectrics leads to degraded channel mobility. Feverish research activities have now been taken on high-mobility channel materials.

It is imperative to have atomically smooth interfaces between high \( \kappa \) gate dielectrics and high-mobility channels such as Si–Ge alloys, Ge, and III–V compound semiconductors (GaAs, InSb, and their related compounds). A low interfacial density of states (\( D_{it} \)) and low electrical leakage current densities are essential in these heterostructures. The III–V’s have much higher electron mobilities than Si, Ge, and their alloys [2].

High electron mobility in the III–V’s is an important aspect for building high-speed devices. Semi-insulating substrates, not available in Si and Ge, will reduce cross talks between high-speed signal lines in dense circuits. A mature compound semiconductor MOS technology with electron mobilities at least 10 times higher than that in Si and with dielectrics having \( \kappa \) several times higher that that of \( \text{SiO}_2 \) would certainly enable the electronic industry to continue pushing its new frontiers for a few more decades. Furthermore, bandgap engineering and direct bandgaps, not available in Si-based material systems, provide...
novel designs and make highly performed integrated optoelectronic circuits of combining MOS and photonic devices a reality. Intensive efforts, including anodic treatment, thermal, and plasma oxidation of GaAs surfaces, and deposition of dielectrics (such as SiO₂, Si₃N₄, Al₂O₃, Ga₂O₃, etc.) on GaAs, failed to give electrically and thermodynamically stable insulators on GaAs with a low $D_{it}$, one of the key challenges in the III–V devices over the past four decades[3]. The puzzle was finally solved with a discovery of UHV (ultra high vacuum) deposition of Ga₂O₃(Gd₂O₃) [4] and pure Gd₂O₃ [5] dielectric films on GaAs surfaces. With such novel gate dielectrics, for the first time MOS diodes have shown inversion and accumulation with a low $D_{it}$ (≤10¹¹ cm⁻²V⁻¹). Subsequent employment of Ga₂O₃ (Gd₂O₃) as a gate dielectric along with an ion implantation process led to the demonstration of the first inversion-channel GaAs MOSFETs in both $n$- and $p$-configurations [6,7] and InGaAs MOSFET in $n$-configuration [8]. Depletion mode (D-mode) devices with negligible drain current hysteresis and drift, a must for manufacturing, have been achieved [9]. More recently, a low $D_{it}$, low leakage current, as well as a D-mode device have also been reported using atomic layer deposition (ALD) Al₂O₃ grown on GaAs [10–12].

In this paper, we discuss mainly the work of our research groups on the high $\kappa$ dielectrics on GaAs and InGaAs, particularly the interface-related structural, chemical, and electrical properties. Our recent results on the perfected nanothick single crystal oxide grown on Si are also reviewed.

2. Ga₂O₃(Gd₂O₃) UHV grown on GaAs and InGaAs, and thermodynamic stability

2.1. Electrical characteristics

Ga₂O₃(Gd₂O₃) has first been shown to passivate GaAs and then successfully to several other III–V’s including AlGaAs, InGaAs, and InP. Systematic post-annealing studies of varying temperatures (from 450 °C to 700 °C), and gas species (He, O₂, N₂, and forming gas in a quartz tube furnace) were carried out in MOS diodes with the oxide deposited mostly on InGaAs. Substantial reduction of problematic features of frequency dispersion and voltage hysteresis was achieved. Leakage current densities of $\sim$10⁻⁸ to 10⁻⁹ A/cm² at fields up to 4 MV/cm, a $\kappa$ value of ~13, and a $D_{it}$ value in the range of 4–9×10¹⁰ cm⁻²V⁻¹ were obtained [13].

In addition, annealing in a reducing gas stream resulted in a preferred decrease of $D_{it}$ as opposed to annealing in an oxidizing gas. However, the forming gas (15% H₂ in a N₂ gas mixture) anneal at 450 °C may have overly reduced the oxides, and adversely increased $D_{it}$ to 10¹³ cm⁻²V⁻¹. The forming gas anneal at 375 °C has effectively reduced the voltage hysteresis to 0.1–0.2 V. A combination of a He anneal at 600 °C with a forming gas anneal at 375 °C has been found to achieve best electrical performance for Ga₂O₃(Gd₂O₃), and is recommended to be incorporated in the III–V MOSFET processing.

Note that in the fabrication of MOS diodes Ga₂O₃(Gd₂O₃) has been exposed to air, thus absorbing moisture. Better electrical properties may be obtained if air-exposure for the oxide can be avoided.

2.2. High temperature thermodynamic stability of Ga₂O₃(Gd₂O₃)/GaAs [14,15]

The electron mobility is strongly affected by the interfacial scattering and degrades rapidly with increasing roughness. The Ga₂O₃(Gd₂O₃)/GaAs interfacial roughness has to be less than a few Å for achieving high device performance in inversion-channel GaAs MOSFET (and in D-mode devices to a lesser degree), as witnessed in the perfected SiO₂–Si interface. The as-deposited interface is atomically smooth with a roughness of $\leq$0.2 nm. It was roughened in a high temperature (N750 °C) annealing. This is detrimental since the annealing was inevitably needed to activate the ion implantation for ohmic

![Fig. 1. High resolution cross-sectional TEM picture of Ga₂O₃(Gd₂O₃) on GaAs annealing in UHV system. The inset is a low angle X-ray reflectivity from the same sample, with experimental data (dots), and a theoretical fit (line).](image1)

![Fig. 2. Leakage current density $J$ (A/cm²) vs $E$ (MV/cm) for Ga₂O₃(Gd₂O₃)/GaAs samples in different thermal processes (sample A was in-situ annealed, while sample B was air-exposed and UHV annealed). The inset shows C–V curves of sample B, after two-frequency corrections.](image2)
contacts at source and drain regions for device fabrication [6–8]. Ga2O3(Gd2O3) absorbs moisture when exposing to air [16]. In fact, any oxide absorbs water and forms hydro-oxides, including SiO2. It is the hydro-oxides, which react with GaAs during annealing at elevated temperatures, resulting in rough interfaces. Ga2O3(Gd2O3) should be thermodynamically stable with GaAs at ∼750 °C or above.

Dwelling at 300 °C for 30 min in UHV has evidenced the removal of moisture out of the air-exposed sample, as shown from a rapid increase of the amount of H2O detected using a residual gas analyzer. The consequent annealing to high temperatures places GaAs to be adjacent to hydro-oxide free Ga2O3(Gd2O3). The values of the roughness of the oxide surface and the interface between the oxide and GaAs have been obtained from the X-ray reflectivity, as illustrated in the inset of Fig. 1, showing a well-behaved fringe pattern. An interfacial roughness of <0.2 nm was calculated using a theoretical fitting model. Fig. 1 shows a cross-sectional high-resolution transmission electron microscopy (HRTEM) picture of the sample, in which the oxide remains amorphous. The oxide thickness measured by the TEM is in agreement with the X-ray reflectivity data. A sharp transition from GaAs to Ga2O3 (Gd2O3) was observed. Even after being exposed to air for more than 100 days and absorbing water vapor, the hydro-oxides in the film were driven out with the 300 °C annealing in UHV.

A leakage current density of Ga2O3(Gd2O3) on GaAs is 10−8 to 10−9 A/cm2 at low gate voltages with the electrical breakdown fields of 4 MV/cm (Fig. 2). C−V curves were obtained with frequencies varying from 1 kHz to 1 MHz and the dispersion in the C−V curves of different frequencies was due to the equivalent circuit of complex impedance (inset of Fig. 2). Capacitances were calculated by the four-element model for different pairs of frequencies. The dielectric constant of Ga2O3(Gd2O3) is calculated to be about 15. The Dit was estimated to be less than 1011 cm−2eV−1 using the Terman method.

Similar results in terms of low Dit, low leakage currents, and high κ value have been obtained in a high temperature anneal in a nitrogen-flow tube furnace (non-UHV). Again, a dwell at 300 °C proves to be necessary [15].

The attainment of a smooth interface between Ga2O3(Gd2O3) and GaAs, even after high temperature annealing for activating implanted dopant, is a must to ensure the low Dit and to maintain a high carrier mobility in the channel of the MOSFET. Our results have provided a critical step for implementing an inversion-channel GaAs MOSFET.

3. ALD Al2O3 on InGaAs — mechanism of unpinning the Fermi level [11,12]

The work presented here has been taken to investigate the mechanism of III–V surface passivation by studying the interfacial compositional, electrical, and structural characteristics of the ALD Al2O3/III–V (InGaAs) heterostructures. The high-resolution X-ray photoelectron spectroscopy (XPS) using synchrotron radiation has detected no residual arsenic oxides in the oxide nor at the oxide/InGaAs interface after the deposition of ALD Al2O3. The native arsenic oxide, As2O3, on top of the...
MBE grown InGaAs after being exposed to air was revealed using XPS. After the ALD process, a small amount of As₂O₅ (note that not As₂O₃) was found to be on the Al₂O₃. The removal of arsenic oxides from the oxide/InGaAs heterostructures ensures the effective passivation (i.e. Fermi-level unpinning), with a $D_{it}$ of $\sim 10^{12}$ eV cm$^{-2}$ deduced from the $C-V$ measurements (inset of Fig. 3). $J-E$ curves show a leakage current density of about $10^{-8}$ to $10^{-9}$ A/cm$^2$ at biasing fields of $b = 3$ MV/cm for both as-deposited and post-annealing samples (Fig. 3). HRTEM reveals a smooth interface and a sharp transition between the oxide and InGaAs in both the as-deposited and annealed conditions (not shown).

Two samples, Al₂O₃/In₀.₁₅Ga₀.₈₅As/GaAs and native oxides/In₀.₁₅Ga₀.₈₅As/GaAs, were used for the XPS investigation with the latter served as a reference (Fig. 4). The As 3d spectra for the as-grown Al₂O₃/In₀.₁₅Ga₀.₈₅As/GaAs (top of Fig. 4) showed a small, but a very profound peak of As₂O₅. The peak quickly disappeared with a slight Ar$^+$ sputtering, indicating a very small amount of arsenic oxides on top of the as-grown sample. There was no detection of any arsenic oxides during the continuous sputtering. After the removal of Al₂O₃ with sputtering, the peaks belonging to InGaAs were revealed. In comparison, the native oxide on the reference sample was found to be As₂O₃ (bottom of Fig. 4) different than the arsenic oxide on top of Al₂O₃ after ALD deposition is As₂O₅; (ii) there is no detectable residue of arsenic oxides within the Al₂O₃ and at the Al₂O₃/InGaAs interface; and In₂O₃ and Ga₂O₃, residues of the native oxide, were detected at the interface due to their higher thermal stability.

In conclusion, we have achieved good electrical properties in ALD Al₂O₃/InGaAs heterostructures without any surface preparation such as HF dip prior to the Al₂O₃ deposition or post-thermal treatment such as annealing in O₂ at $\sim 600$ °C. The high-resolution XPS using synchrotron radiation has shown that no residual arsenic oxides exist at the interface of the oxide/InGaAs heterostructures, without post-deposition annealing in O₂.

Fig. 5. $D_{it}$'s determined using the Terman method for ALD Al₂O₃/InGaAs and for UHV deposited Ga₂O₃(Gd₂O₃) on GaAs.

Fig. 6. X-ray theta two-theta scan along Si (111) surface of (111) γ-Al₂O₃ film 3.8 nm thick and the mosaic scan of the γ-Al₂O₃ (222) peak [19].

Fig. 7. Cross-sectional TEM image and electron diffraction pattern of a 3.8 nm γ-Al₂O₃ film, showing a sharp interface and smooth surface. The electron diffraction pattern indicates that the film is well aligned with Si substrate. The in-plane electron diffraction pattern of the 3.8 nm γ-Al₂O₃ film is shown in the inset.
4. High-quality nano-thickness single crystal oxides on Si (111) [17,18]

Hetero-epitaxy between oxides and semiconductors is always fascinating in science and important in technology. For example, growth of single crystal GaN on sapphire is a backbone for producing blue lasers and LED’s, a basis for future lighting industry. Epitaxial growth of insulators on Si is another example, which may find applications in high $\kappa$ dielectrics for the Si industry, an urgent technological issue. A subsequent single-crystalline growth of other semiconductors such as GaN or GaAs on these single crystal insulators may integrate high-power microwave devices or lasers with the most advanced Si-based electronic devices.

4.1. $\gamma$-Al$_2$O$_3$ [17]

Single crystal Al$_2$O$_3$ films have been epitaxially grown on Si (111) substrates despite a huge lattice mismatch. The structural and interfacial studies carried out by X-ray diffraction (Fig. 6), X-ray reflectivity, and HRTEM (Fig. 7), with the initial epitaxial growth observed by in-situ reflective high-energy electron diffraction show that the oxide films as thin as 3.8 nm have the cubic $\gamma$-phase with a very uniform thickness and a highly structural perfection. The film surface is very smooth of 0.12 nm in roughness and the oxide/Si interface is atomically sharp. The $\gamma$-Al$_2$O$_3$ films are well aligned with Si substrate with an orientation relationship of Si (111) // Al$_2$O$_3$ (222), Si [220] // Al$_2$O$_3$ [440].

4.2. Cubic Sc$_2$O$_3$ [18]

Sc$_2$O$_3$ is attractive as an alternative gate dielectric for Si due to its relatively high dielectric constant of $\sim$ 14, large bandgap of $\sim$ 6 eV, and thermodynamic stability with Si. Interestingly, high-quality single-crystal Sc$_2$O$_3$ films a few nano-meter thick have been grown epitaxially on Si (111) despite a huge lattice mismatch. The films were electron beam evaporated from a Sc$_2$O$_3$ target. Structural studies were carried out by X-ray diffraction (Fig. 8) and reflectivity, HRTEM (Fig. 9), and medium energy ion scattering (MEIS), with the initial epitaxial growth monitored by in-situ reflection high-energy electron diffraction (RHEED). The films have shown a high-intensity and persistent thickness fringe oscillations around the Sc$_2$O$_3$ (222) and (444) diffraction peak (Fig. 8) and narrow rocking curves of Sc$_2$O$_3$ (222) and (444). These films were of the bulk bixbyite cubic phase with high structural perfection, sharp interface with Si, and the (111) axis of the oxide films parallel to the substrate normal. The cone scans of the Sc$_2$O$_3$ {440} and Si {220} diffraction peaks about the surface normal indicated a 60° symmetric rotation of the film with respect to the substrate. The film surfaces are very smooth and the oxide/Si interfaces are atomically sharp with a low average roughness of 0.06 nm. The films are well aligned with the Si substrate with an orientation relationship of Si (111) // Sc$_2$O$_3$ (111), and an in-plane epitaxy of Si [1¯10] // Sc$_2$O$_3$ [101].

5. Conclusion

The interplay between science and technology in nano-meter scale is critical in solving the urgent issues of high $\kappa$ gate dielectrics on high-mobility channel materials. The ability of controlling the growth and interfaces of ultra-thin dielectric films on the III–V compound semiconductors by ultrahigh vacuum (UHV) physical vapor deposition has led to comprehensive studies of gate stacks employing high $\kappa$ gate oxide Ga$_2$O$_3$(Gd$_2$O$_3$). These oxides as gate dielectrics on GaAs and InGaAs have been shown to possess a low interfacial density of states ($D_{it}$), thus solving a problem which has puzzled researchers for almost four decades. The electrical, thermal, and structural properties of these novel oxides and their interfaces with GaAs are reviewed. Particularly the achievement of low $D_{it}$ and thermodynamic stability upon high temperature annealing is reviewed. The mechanism of Fermi-level
unpinning in atomic layer deposition (ALD) Al2O3 on InGaAs was studied and understood.

The understanding of abrupt interfaces and controlled microstructures achieved in this work can be used to elucidate critical issues of materials integration in the complementary metal-oxide-semiconductor (CMOS) process. In nano electronic devices, surfaces and interfaces of semiconductors with dielectric insulators such as oxides always play critical roles in determining properties of materials and performance of devices.

Sc2O3 and Al2O3 significantly have different crystal structures, different bonding, and lattice constants than Si. It is intriguing that a highly ordered epitaxial growth was obtained with these unusually large mismatches. We have recently successfully grown single crystal GaN on these two nano-thick oxides.

Diffraction, reflectivity, and X-ray photoelectron spectroscopy using synchrotron radiation have proved to be pivotal in understanding many interfacial structural and electronic properties, including the unpinning mechanism in the high κ gate dielectrics on the III–V compound semiconductors.

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