Structural and electrical characteristics of Ga$_2$O$_3$(Gd$_2$O$_3$)/GaAs under high temperature annealing

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Atomic smooth Ga$_2$O$_3$(Gd$_2$O$_3$)/GaAs interface with low interfacial density of states and low electrical leakage currents have been achieved after the heterostructures were air exposed and tailor annealed to $\sim$750 $^\circ$C. The heat treatments, with annealing at an intermediate temperature of $\sim$300 $^\circ$C as a necessary step, were carried out under ultrahigh vacuum (UHV) and via standard rapid thermal annealing with flow of pure nitrogen gas. Furthermore, the oxide remains amorphous and minimal interfacial reaction occurred between the oxide and substrate, critical aspects for device performance. Studies using x-ray reflectivity and high-resolution transmission electron microscopy show that the interfacial roughness is $<$0.2 and $<$0.4 nm for annealing under UHV and non-UHV, respectively. Electrical measurements on the metal-oxide-semiconductor diodes have exhibited low leakage currents ($10^{-8}$–$10^{-9}$ A/cm$^2$), a dielectric constant of $\approx$14, and a low interfacial density of states ($D_n$) of $<10^{12}$ cm$^{-2}$ eV$^{-1}$. © 2006 American Institute of Physics. [DOI: 10.1063/1.2386946]

I. INTRODUCTION

III-V compound semiconductors offer the advantages of high electron mobilities, rich band gap engineering, and high breakdown fields and thus are expected to outperform silicon in certain metal-oxide-semiconductor (MOS) applications such as high-speed and high power devices. In contrast to the present commercially available III-V metal-semiconductor field-effect transistors (MESFET’s) and high electron mobility transistors (HEMT’s), which exhibit small forward gate voltages limited by the Schottky barrier heights, the III-V MOSFET’s feature a much larger logic swing which gives a greater flexibility for digital integrated circuit (IC) designs and higher current gain cutoff frequency.1,2

One key challenge in the III-V technology was to identify thermodynamically stable insulators on the III-V’s that give a low interfacial density of states ($D_n$) and a low leakage current.3 The intensive efforts in questing for such competitive insulator/III-V systems have finally yielded fruitful results with the discovery of high $\kappa$ dielectric Ga$_2$O$_3$(Gd$_2$O$_3$) on GaAs (Refs. 4 and 5) and atomic layer deposition (ALD) Al$_2$O$_3$ on InGaAs,6,7 in which a low electrical leakage current and a low $D_n$ have been achieved. The employment of Ga$_2$O$_3$(Gd$_2$O$_3$) as a gate dielectric along with an ion implantation and rapid thermal annealing (RTA) for activating implanted ions has led to the demonstration of the first inversion-channel $n$- and $p$-GaAs MOSFETs (Refs. 8 and 9) and InGaAs $n$-MOSFET.10

The oxide-GaAs interface, however, was roughened due to high temperature (750 $^\circ$C) annealing (either via RTA or other methods) during the MOSFET’s fabrication. The high temperature annealing was required to activate the ion implantation for Ohmic contacts at source and drain regions. It was found that Ga$_2$O$_3$(Gd$_2$O$_3$) absorbs water with air exposure,11 and the hydro-oxides, not the pure Ga$_2$O$_3$(Gd$_2$O$_3$), reacted with GaAs resulting in rough surfaces and interfaces. The hydroxide formation is common for transition metal and more so for rare earth oxides upon air exposure, and that affects the stability and reduces the reliability of the oxides for device performance.

Thermodynamically, pure Ga$_2$O$_3$(Gd$_2$O$_3$) is stable with GaAs at temperatures higher than 800 $^\circ$C. Indeed, by removing water from air-exposed oxide with a low-temperature annealing prior to heating to high temperatures (not RTA) in ultrahigh vacuum (UHV), an atomically smooth Ga$_2$O$_3$(Gd$_2$O$_3$)/GaAs heterointerface has been achieved.12 The interfacial roughness is less than 0.2 nm, close to the value in the perfected SiO$_2$–Si interface. Furthermore, Ga$_2$O$_3$(Gd$_2$O$_3$) remains amorphous, and a low leakage current and a low $D_n$ have been demonstrated.12

For fabricating devices, however, a non-UHV annealing is preferred over the UHV approach for practical reasons. Thermodynamically, water may also be driven out of Ga$_2$O$_3$(Gd$_2$O$_3$) when the sample is heated under a no-water

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environment, such as a furnace (tube type) or RTA flowing with high-purity nitrogen or inert gases. Also, RTA has been employed in this work, since it is advantageous for improving activation efficiencies, decreasing dopant lateral diffusion, and sharpening doping profiles. These are important for inversion-channel GaAs MOSFET’s, in which the source and drain regions are ion implanted and activated in high temperature to define the device channel and decrease the contact resistance. The short annealing time at high temperatures, typically several seconds, and rapid ramping rates are employed.

In this work, under a tailored heating procedure, air-exposed Ga2O3(Gd2O3)/GaAs samples annealed in a commercial RTA machine under non-UHV were shown to achieve excellent structural and electrical properties, similar to what was obtained with samples annealed in UHV. Annealing the samples at 300 °C for 10 min followed by RTA to high temperatures of 750 °C under pure nitrogen flow has revealed that the interface between Ga2O3(Gd2O3) and GaAs remains intact with the interfacial roughness less than 0.4 nm, slightly larger than the interfacial roughness (<0.2 nm) for samples under UHV annealing again with a dwell at 300 °C. Moreover, Ga2O3(Gd2O3) remains amorphous, an important aspect for high κ gate dielectrics. J-E [current density–field (voltage divided by oxide thickness)] and C-V (capacitance-voltage) measurements showed that leakage currents of 10⁻⁸–10⁻⁹ A/cm² through the oxide and Dµ’s remain low of <10¹² cm⁻² eV⁻¹.

An annealing at 750 °C may activate <10% of the implanted Si, which gives a doping level of slightly less than 1×10¹⁵ cm⁻³. As a consequence, it is reasonable to obtain a contact resistance in the 10⁻⁵ Ω cm² range, as was reported in Refs. 14 and 15. An annealing at higher temperature may activate a higher percentage of the implanted Si, thus giving a lower contact resistance. In the present GaAs MOS devices, the Ohmic contact resistance is not the most serious issue while the oxide/GaAs interface and the integrity of the oxide are. Higher activation temperatures may recrystallize the amorphous gate oxide, thus dramatically increasing the gate leakage. Also, the oxide/GaAs interface may be damaged and Dµ may increase. These may deteriorate the device performance more than the influence of the contact resistance. The activation annealing process was not optimized in the present work. Nevertheless, the contact resistance will have to be made lower when the inversion-channel GaAs MOSFET begins to show decent drain currents and transconductance. The efforts are being taken towards lowering the contact resistance and at the same time maintaining smooth oxide/GaAs interfaces and preventing recrystallization of the oxide.

II. EXPERIMENT

A. Growth

Deposition of GaAs epilayers and oxide films as the gate dielectrics was carried out in a multichamber UHV system, which includes a solid-source GaAs-based III-V semiconductor molecular beam epitaxy (MBE) chamber, two arsenic-free UHV oxide deposition chambers, and UHV wafer transfer modules. The growth sequence starts with the GaAs epilayer, and then transferring the wafer in situ to the oxide chamber for depositing the dielectric oxide under a vacuum of 10⁻¹⁰ Torr. The oxide was electron beam evaporated from a single crystal Ga2O3(Gd2O3) garnet. The substrate temperature during the oxide growth was held at about 550 °C. The samples were removed from the multichamber MBE system and Si3N4 layers were deposited on the back side of the wafer to prevent arsenic from evaporation during high temperature annealing.

B. Heat treatments

Samples A1 and A2 were cut from the same wafer, which was removed from the UHV system and air exposed. They were RTA under flow of pure N2 gas, but in different heating procedures, as shown in Table I, with A1 being RTA directly to 750 °C (and staying there for 30 s and then cooling down to room temperatures) and A2 RTA to 300 °C, dwelled there for 10 min, and then RTA to 750 °C. For comparison, samples B1, B2, and B3 were annealed in UHV under various conditions. After oxide growth, samples B1 and B2 were moved out of the UHV system, exposed to the

### Table I. X-ray reflectivity and electrical studies on Ga2O3(Gd2O3)/GaAs, with Tox as the determined oxide thickness.

<table>
<thead>
<tr>
<th>No.</th>
<th>Tox (nm)</th>
<th>Thermal process</th>
<th>Surface roughness (nm)</th>
<th>Interfacial roughness (nm)</th>
<th>k value</th>
<th>Leakage (a/cm²) at 1 MV/cm</th>
<th>Dµ (eV⁻¹ cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>30</td>
<td>Exposed to air, RTA directly to 750 °C, 30 s with N2 flow</td>
<td>Very rough</td>
<td>Very rough</td>
<td>x</td>
<td>2.8 × 10⁻⁹</td>
<td>x</td>
</tr>
<tr>
<td>A2</td>
<td>30</td>
<td>Exposed to air, dwelled at 300 °C for 10 min, and RTA to 750 °C in 30 s, all under N2 flow</td>
<td>0.6</td>
<td>0.4</td>
<td>13.8</td>
<td>4.2 × 10⁻⁹</td>
<td>(2–3) × 10¹¹</td>
</tr>
<tr>
<td>B1</td>
<td>37.7</td>
<td>Exposed to air, directly annealing to 750 °C in UHV</td>
<td>0.93</td>
<td>0.68</td>
<td>16.8</td>
<td>5.8 × 10⁻⁹</td>
<td>(2–3) × 10¹¹</td>
</tr>
<tr>
<td>B2</td>
<td>25</td>
<td>Exposed to air, dwelled at 300 °C for 30 min prior to annealing to 750 °C in UHV</td>
<td>0.47</td>
<td>0.14</td>
<td>13.7</td>
<td>4.1 × 10⁻⁹</td>
<td>(2–3) × 10¹¹</td>
</tr>
<tr>
<td>B3</td>
<td>26.1</td>
<td>In situ annealing directly to 750 °C in UHV</td>
<td>0.64</td>
<td>0.17</td>
<td>14.3</td>
<td>5.1 × 10⁻⁹</td>
<td>(2–3) × 10¹¹</td>
</tr>
</tbody>
</table>

Reference 12.
atmosphere for more than 100 days, and put back to UHV. B1 was heated up directly to above 750 °C, while B2 was ramped up to 300 °C and dwell there for 30 min prior to being heated up to above 750 °C. B3 was in situ directly heated to above 750 °C in UHV. Samples A1 and A2 are to be compared with B1 and B2, respectively, with the former being treated under non-UHV and the later under UHV.

C. Structural analysis

Structural and morphological probing tools such as x-ray reflectivity (XRR) and cross-sectional high-resolution transmission electron microscopy (HRTEM) have been employed. XRR under grazing incidence conditions is a simple, yet useful technique to study the electron density, thickness, surface, and interfacial roughness of the oxide/GaAs heterostructures without destroying the samples. The measurements were performed using Cu Kα radiation in a standard Huber four-circle x-ray diffractometer operated at 50 kV and 200 mA. The incident light was monochromatized by a flat Ge (111) crystal and two sets of slits were used to eliminate Cu Kα2 and a wave-vector resolution in the scattering plane was 0.015 nm⁻¹. The theory of specular reflectivity is based on the recursive formalism of Parratt. To determine physical parameters of the film such as interfacial roughness, thickness, and electron density, the reflectivity data were fitted with the BEDE REF5 MERCURY code.

HRTEM specimens were prepared with mechanical polishing, dimpling, and ion milling using a Gatan PIPS system operated at 3 kV. The TEM sample analytical work was performed using a Philips Tecnai-20 FEG-type TEM. The oxide film thickness was also determined using spectral ellipsometry.

D. Electrical characteristics

Studies of leakage currents and \( D_q \)'s were carried out on Au/Ga\(_2\)O\(_3\)/(Gd\(_2\)O\(_3\))/GaAs MOS diodes, with a dot size of 0.1 mm in diameter. \( J-E \) and \( C-V \) characteristics were measured using Agilent 4156C and 4284, respectively. \( J \) is the current density with electrical currents divided by the area of the metal dot and \( E \) is the electrical field with biasing voltages divided by the oxide thickness. \( C-V \) curves were measured with frequency varying from 1 to 500 kHz.

The room temperature high frequency Terman method was used to estimate the minimum \( D_q \)'s, which were given in Table I. From the difference between the measured \( C-V \) data and the theoretical curve for \( D_q=0 \), the \( D_q \)'s were deduced using the formula of \( D_q = (C_\text{ox}/q)[(dV_G/d\phi_f) - 1] - (C_q/q) \), where \( C_\text{ox} \) is the oxide capacitance per unit area (F/cm²), \( q \) magnitude of electron charge (1.6 × 10⁻¹⁹ C), \( V_G \) the experimental gate voltage (V), \( \phi_f \) the surface potential of semiconductor (V), and \( C_q \) was the semiconductor capacitance (F). The method relies on a high frequency \( C-V \) measurement at a frequency sufficiently high that interfacial traps are assumed not to respond with the ac probing signal, therefore, not contributing any capacitance. However, they do respond to the slowly varying dc gate voltage and cause the high frequency \( C-V \) curve to stretch out along the gate voltage axis as interface trap occupancy charges with gate bias.

III. RESULTS AND DISCUSSION

XRR measurements on samples A1, A2, B1, B2, and B3 are shown in Figs. 1(a)–1(e). Oxide thickness and roughness of the oxide surface and Ga\(_2\)O\(_3\)/(Gd\(_2\)O\(_3\))/GaAs interface are listed in Table I. The interfacial roughness of A2 is 0.4 nm, which is larger than those of B2 and B3, and less than that of B1. This indicates that the tailored heat treatment of dwelling the sample at 300 °C before RTA it to high temperature ensures the smooth oxide/GaAs interface and oxide surface. In comparison, samples such as A1 and B1 without being dwelled at low temperatures exhibited rough interfaces and surfaces, regardless under UHV or not. The roughness is smaller for samples annealed in UHV, while A1 became very rough, as shown in Fig. 1(a). The ramping rate of heat treatments under the UHV setup is not as fast as that using commercial RTA. Therefore, moisture may be allowed to be driven out of the samples under the UHV annealing.

Micrographs of cross-sectional HRTEM on samples A2, B1, B2, and B3 are shown in Figs. 2(a)–2(d). The oxide thickness measured by TEM is in agreement with that from x-ray reflectivity data. A sharp transition from GaAs to Ga\(_2\)O\(_3\)/(Gd\(_2\)O\(_3\)) after high temperature annealing without interfacial layers was observed in samples A2, B2, and B3.
HRTEM studies on as-deposited Ga2O3(Gd2O3)/GaAs are routinely carried out and were reported earlier,\textsuperscript{11,19} in which a sharp and smooth oxide/semiconductor interface has been shown and is expected. The smoothness in surface and the interface of the oxide/GaAs heterostructure is also revealed in its x-ray reflectivity study\textsuperscript{19} of the oscillatory behavior and a slow decline in the diffraction intensity with the increase of the x-ray incident angle.

In contrast, a fast declination in the intensity and no oscillation in the reflectivity curve shown in Fig. 1(a) for A1 indicate a rough surface and interface, which was caused by the reaction between Ga2O3(Gd2O3) containing hydro-oxides with GaAs. This is anticipated from what was learned in our earlier work of the UHV annealing on Ga2O3(Gd2O3)/GaAs.\textsuperscript{12} Air-exposed Ga2O3(Gd2O3) needs to be dehydrated prior to high temperature annealing in order to achieve atomically smooth interface.

The results from sample A1 revealed the difficulties encountered in the fabrication of inversion-channel GaAs MOSFET using Ga2O3(Gd2O3) as the gate dielectric without a cap layer for protection. The rough interface when annealing under non-UHV is mainly caused by the penetration of water moisture in the air-exposed oxides. Capacitance-voltage measurements on this sample showed that the capacitance does not vary with the applied voltages. Thus, the Fermi level is pinned and no meaningful interface state density can be deduced.

A small interfacial roughness of \(<0.2\,\text{nm}\) has been obtained in the interface of Ga2O3(Gd2O3)–GaAs of both B2 and B3. After the high temperature (>750 °C) annealing process, reflection high-energy diffraction (RHEED) patterns and x-ray diffraction (not shown) indicate that the samples remain amorphous. The results of smooth interface, low leakage currents, and low \(D_i\) are consistent with the thermodynamic stability of Ga2O3(Gd2O3)/GaAs at high temperatures.

In the following, we would focus on the electrical characteristics of sample A2, since the heat treatment in A2 is readily adapted for a practical device application. Figure 3 is a \(J-E\) curve for A2 showing a leakage current density of about \(10^{-8}-10^{-9}\,\text{A/cm}^2\) at low gate voltages. The low leakage current also reveals the high quality and the integrity of Ga2O3(Gd2O3) after air exposure and high temperature annealing. Note that A2 was air exposed and heat treated under flowing nitrogen gas (not in UHV). The electrical breakdown fields are roughly 6 MV/cm.

The dispersion in the \(C-V\) curves for sample A2 under different frequencies was due to a circuit of complex impedance, as shown in Fig. 4. The operation in accumulation, depletion, and inversion is evident with frequencies. The MOS diodes of A2 show the \(C-V\) curves expected for an unpinned oxide/GaAs interface. The dielectric constant of Ga2O3(Gd2O3) is calculated to be about 14, comparable to the values obtained in B2 and B3 with similar oxide thicknesses.
Figure 5 shows the distribution of $D_{it}$ as a function of $E_c - E$ ($E_c$ is the edge of conduction band) for sample A2, in which $D_{it}$ at the midgap was estimated to $\sim (2-4) \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$, similar to the value obtained in the as-grown sample. The $D_{it}$ value did not increase with the ex situ high temperature annealing.

When the $D_{it}$’s are low in the range of $10^{11} \text{cm}^{-2} \text{eV}^{-1}$ or below, the Terman method may not give an accurate determination of the interfacial density of states. From the distribution of $D_{it}$’s as a function of $E_c - E$ for all measured samples, it was found that $D_{it}$’s are all in the low $10^{11} \text{cm}^{-2} \text{eV}^{-1}$. It is difficult to distinguish the difference among them, even though the interface of sample B1 is rougher than that of samples A2, B2, and B3. However, the electrical measurement is more sensitive in detecting defects and/or traps, which are not detectable using cross-sectional HRTEM and XRR.

IV. CONCLUSION

The results have demonstrated that the intermediate annealing at 300 °C in a N2 flowing environment or under UHV is effective in reducing the hydroxides, thus giving the high temperature thermodynamic stability of Ga2O3/(Gd2O3)/GaAs. Furthermore, the oxide remains amorphous and minimal interfacial reaction occurred between the oxide and substrate, ensuring the excellent electrical properties of low $D_{it}$, low leakage currents, and high dielectric constant.

The attainment of a smooth interface between the gate dielectric and GaAs after high temperature annealing is critical for achieving low $D_{it}$ and maintaining a high carrier mobility in the MOSFET’s channel. The work here has extended our earlier results using UHV annealing to more commonly used non-UHV approach of RTA (under pure N2 gas environment). The findings enable fabrication of high-performance inversion-channel GaAs-based MOSFET’s.

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