Progress in silicon-based quantum computing

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We review progress at the Australian Centre for Quantum Computer Technology towards the fabrication and demonstration of spin qubits and charge qubits based on phosphorus donor atoms embedded in intrinsic silicon. Fabrication is being pursued via two complementary pathways: a ‘top-down’ approach for near-term production of few-qubit demonstration devices and a ‘bottom-up’ approach for large-scale qubit arrays with sub-nanometre precision. The ‘top-down’ approach employs a low-energy (keV) ion beam to implant the phosphorus atoms. Single-atom control during implantation is achieved by monitoring on-chip detector electrodes, integrated within the device structure. In contrast, the ‘bottom-up’ approach uses scanning tunnelling microscope lithography and epitaxial silicon overgrowth to construct devices at an atomic scale. In both cases, surface electrodes control the qubit using voltage pulses, and dual single-electron transistors operating near the quantum limit provide fast read-out with spurious-signal rejection.

Keywords: quantum computer; silicon; single electron transistor; charge qubit; spin qubit

1. Introduction

It is widely believed that solid-state systems have much to offer in the search for a scalable quantum computer (QC) technology. One of the most advanced proposals is based on superconducting qubits (Shnirman \textit{et al.} 1997), where coherent control of

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a qubit has been demonstrated and decoherence times measured (Nakamura et al. 1999; Vion et al. 2002; Yu et al. 2002; Martinis et al. 2002), with the first evidence for qubit coupling having been reported recently (Pashkin et al. 2003). In these systems, a macroscopic number of electrons condense into a single (superconducting) ground state, which forms the basis of the qubits. Semiconductor schemes are also significant—in particular those based on silicon–metal-oxide-semiconductor technology, due to their compatibility with existing technology. In Kane’s (1998) scheme (figure 1a) the qubits are formed from the very-long-lived nuclear spins of single phosphorus dopants in an Si host crystal, and manipulated by external surface gates and radio-frequency (RF) magnetic fields. Qubit coupling is via the hyperfine and

electron-exchange interactions, requiring qubit spacing of ca. 20 nm. A complementary Si–SiGe:P architecture has been proposed using exchange-coupled electron spin states as qubits (Vrijen et al. 2000), with increased qubit spacing (ca. 100 nm) in the Si–SiGe structure. Although single-spin read-out has yet to be demonstrated in semiconductors, recent experiments have shown that the electron spin $T_2$ lifetimes in $^{28}$Si at electron densities corresponding to several tenths of a micron spacing exceed 60 ms at low temperatures (Tyryshkin et al. 2003), with the possibility of even longer (ca. 1 s) coherence times at millikelvin temperatures. It is important to realize that the work of Tyryshkin et al. is for a bulk doped sample, where the decoherence time of a single electron spin in the environment of a large number of uncontrolled spins is measured. Consequently the long decoherence times are constrained to lightly doped samples due to dipole–dipole interactions. However, it is important to realize that in a precisely fabricated quantum computer where all of the qubits and their interactions are controlled with gates, the total spin–spin interactions (exchange and dipole–dipole) are central to the qubit coupling process (albeit slightly more complicated than exchange-only coupling), and therefore in principle do not constitute a decoherence process. One would therefore expect decoherence times for a quantum computer to be of the same order as those for the lightly doped samples, despite the fact that the donor spacing is very much smaller. While the ‘hard’ nanofabrication and measurement of single-buried-atom qubit arrays in silicon have presented significant challenges, this architecture avoids many obstacles to scaling, such as crosstalk between electromagnetic fields of more easily fabricated macroscopic circuits. Beyond the current (and correct) international focus on demonstration of coherence via Rabi oscillations, single-atom qubits have a number of advantages with respect to decisive issues that will determine the viability of a large-scale QC.

Although the electrical detection of single spins has not been achieved, fast single-charge detection is already in place due to pioneering developments in RF-SET technology (Schoelkopf et al. 1998; Aassime et al. 2001). In a spin-read-out scheme proposed by Kane, RF-SETs have been proposed to read out the states of single nuclear and electron spins, by detecting spin-dependent electron tunnelling between adjacent P atoms (Kane 1998; Kane et al. 2000). However, this is a challenging task, complicated by the small (ca. 1 meV) binding energy associated with two electrons of opposite spin on a single P donor in Si ($D^-$ centre). Because of the common read-out technology, we have therefore developed (Hollenberg et al. 2003) an Si:P charge-qubit architecture (figure 1b) which is complementary to the Kane concept, but experimentally accessible now. The quantum logic states correspond to the lowest two states of the single valence electron localized by the double well formed by two donor P atoms. Surface gates allow for qubit preparation ($P-P \rightarrow P-P^+$), external control over the potential barrier height (B gate) and potential symmetry (S gate) for manipulation of localized qubit states ($|0\rangle = |L\rangle$ and $|1\rangle = |R\rangle$), while twin-RF-SETs facilitate qubit initialization and read-out.

Due to its stronger coupling to the environment, the charge qubit will decohere faster than its spin-based counterpart. However, calculated gate-operation times can be as fast as 50 ps (Hollenberg et al. 2003), commensurately faster than the microsecond operation times (Fowler et al. 2003) for spin qubits. Additionally, we have developed a single-shot RF-SET read-out scheme for the charge qubit superposition basis $|0\rangle = (1/\sqrt{2})(|L\rangle + |R\rangle)$, $|1\rangle = (1/\sqrt{2})(|L\rangle - |R\rangle)$ (Greentree et al. 2003), offering the prospect of significantly enhanced coherence times, as found for superconducting
charge qubits in this basis. This read-out scheme is directly extendable to single spin read-out via RF-SETs.

Coupling schemes for the charge qubit have also been proposed (Hollenberg et al. 2003). In the ‘CNOT’ arrangement shown in figure 1d, qubit $Q_1$ acts on the effective barrier height of qubit $Q_2$, and the coupling is primarily given by $\Gamma_{xx}^{(1)} \phi_x^{(2)}$. The effect of moving a charge of 1.0e between the ‘a’ and ‘b’ positions of $Q_1$ (see figure 1d) on the qubit $Q_2$ was calculated with ‘a’ and ‘b’ chosen to be 60 and 30 nm from the barrier centre of $Q_2$, respectively, and was found to give a coupled-qubit operation time of 0.1–1 ns (Hollenberg et al. 2003).

Operational issues aside, the spin- and charge-based Si:P schemes shown in figure 1 (as well as the Si–SiGe:P (Vrijen et al. 2000) and more recent flying qubit proposals (Skinner et al. 2003)) face an identical challenge: placement of individual phosphorus donors within a low-disorder intrinsic-silicon (i-Si) substrate at precise array sites, accurately positioned with respect to the surface control gates and SETs. In this paper we review two contrasting approaches currently being developed to attain this goal, together with the SET measurement techniques required to read out the state of a qubit.

In § 2 we describe a top-down construction approach for which prototype charge-qubit devices have been successfully fabricated (Dzurak et al. 2003). Array sites are defined by top-down lithographic patterning of a resist mask and the donors are implanted through the mask using a keV phosphorus-ion beam. The implantation of P donors is controlled with single-ion accuracy, allowing devices to be configured atom by atom. In § 3 we discuss the use of a twin-SET architecture for correlated detection of single-electron transfer in a device—in particular operation of these devices at the megahertz frequencies required for read-out in both charge- and spin-based qubit schemes. Finally, in § 4 we outline a bottom-up atomic assembly approach (O’Brien et al. 2001; Simmons et al. 2003) that is potentially capable of constructing devices with close to atomic precision. Here scanned-probe lithography of a hydrogenated silicon surface together with epitaxial Si overgrowth is used to construct a buried P array. We review a number of key proving experiments, which show that complete construction of a prototype device by the bottom-up approach is within reach.

2. Top-down fabrication using controlled single-ion implantation

In the conventional microelectronics industry, ion implantation is a standard technique for the incorporation of dopant atoms and is essentially a bulk process involving many dopants. We have recently developed a technique which enables controlled single-ion implantation (Dzurak et al. 2003). Ion-impact detectors, integrated into the devices, are monitored electronically during implantation. When a single ion enters the i-Si substrate, it produces electron–hole pairs that drift in an applied electric field, creating a detectable current pulse for each ion strike. Although discussed here for the construction of QC devices, this technology is applicable to any semiconductor device where accurate control of the dopant number is important.

Figure 2 depicts the technique developed to localize individual phosphorus atoms at the desired qubit array sites for a two-donor device. A nanopatterned ion-stopping resist such as poly(methyl methacrylate) (PMMA) defines the array sites and a low-energy (14 keV) $^{31}$P$^+$ ion beam is used to implant the P dopants to an average depth

of 15 nm below the Si–SiO$_2$ interface, for a 5 nm thick SiO$_2$ layer. Each ion entering the substrate creates $ca.500$ e$^-$/h$^+$ pairs which drift in an internal electric field produced by a bias voltage up to 10 V applied between two detector electrodes. The resulting current is amplified in an external, high-efficiency cooled detector circuit to produce a single pulse for each ion strike. The two aluminium detector electrodes form Schottky contacts which act as back-to-back diodes under bias, restricting the dark current (no $^{31}$P$^+$ beam) to below 100 pA.

Typical data for an incident 14 keV $^{31}$P$^+$ ion beam are shown in figure 2d for an interdigitated electrode array with lateral dimension $ca.100$ µm. Pulses above the noise threshold occur with a frequency consistent with the areal ion dose of $ca.5$ ions ms$^{-1}$ across the active device area and can therefore be unambiguously identified as single-ion strikes. The e$^-$/h$^+$ pair separation mechanism has been modelled using technology computer-aided design (Pakes et al. 2003b) and is found to create a current pulse in 40 ps. The temporal broadening of the peaks in figure 2d results from the time constant of the external circuit.

While semiconductor detectors are well-established (Bertolini & Coche 1968), to our knowledge this is the first use of a detector integrated into a device to precisely control its doping level. Furthermore, the 14 keV data in figure 2d represent the first detection of P$^+$ ions at an energy below 80 keV. This energy resolution is partly due to the presence of a near-intrinsic Si substrate. While critical for Si:P QC devices, the use of intrinsic Si also ensures that the electric field penetrates maximally throughout the sample. To explore the field penetration we have rastered an MeV ion beam across various electrode geometries and monitored the charge collection efficiency at each point (Yang et al. 2002), finding collection efficiencies of $ca.99\%$ at distances up to 10 µm from the electrodes. We can therefore fabricate detector electrodes set many micrometres back from the central nanostructured region where the qubits and control gates are located.

Because of their mass, $^{31}$P$^+$ ions with incident energy 14 keV lose $ca.85\%$ of their initial energy to nuclear stopping events in the substrate, compared with only $ca.20\%$ for light ions such as $^1$H$^+$. The energy available for the creation of e$^-$/h$^+$ pairs is therefore $ca.2$ keV. Because the path taken by each incident ion is different, the exact number of e$^-$/h$^+$ pairs and the resulting current pulse height will vary between events, as seen in figure 2d. To ensure that no ions enter the substrate without detection, the noise level must be kept significantly below the mean pulse height. Using cryogenic-detection electronics we have been able to reduce the effective noise level to an energy equivalent of $ca.1$ keV and expect that a value of 0.1 keV will be possible in the near future, providing greater than 95% confidence that all ions have been detected.

At present we are applying a uniform areal ion dose to our masked substrates, broadly focused over the aperture region, so that ion placement is random between the apertures. For the P–P$^+$ charge-qubit device of figure 1b it is possible that the two implanted ions will have gone down the same aperture, leading to a one-in-two probability of correctly configuring a device with one P atom at each site. Such a yield is sufficient for proof-of-principle experiments on one-qubit devices. For large-scale qubit arrays it will be necessary to direct each ion to its appropriate array site using a $^{31}$P focused ion beam, one of which has recently been installed in the Centre for Quantum Computer Technology.

Figure 2. Electrically registered single-ion implantation. (a), (b) Optical images of detector electrodes. (c) Schematic showing phosphorus implantation through a resist mask. Each ion strike creates an electron–hole plasma, producing a current pulse monitored by on-chip electrodes. (d) Experimental demonstration of single-ion strikes in an i-Si substrate from a 14 keV phosphorus-ion beam. (Reproduced from Dzurak et al. (2003).)

Devices incorporating implanted phosphorus donors, with fully configured surface control gates and dual-read-out SETs have recently been constructed (Dzurak et al. 2003) to study controlled electron transfer between donors. Following the successful achievement of a one-qubit, two-donor-atom implant, initial electrical measurements have concentrated on devices where each donor is replaced by a cluster of phosphorus...
donors. Figure 3a shows such a device containing 100 phosphorus donors in each cluster. A range of such devices spanning the metal–insulator transition is under investigation.

The fabrication of a device such as that shown in figure 3 involves a number of high-resolution electron-beam lithography (EBL) steps, each of which must be aligned to the others to within 20 nm. The process flow proceeds as follows. Firstly, a 5 nm thick SiO$_2$ layer is thermally grown on a near-intrinsic silicon wafer, with a background n-doping level of $10^{12}$ cm$^{-3}$. If single-ion doping control is required, micrometre-scale
aluminium detector electrodes are then deposited on the substrate using ultraviolet lithography. Next, to provide sub-20 nm alignment accuracy between all features on the device, Ti/Pt alignment markers are patterned using EBL. In a second EBL step, two sub-30 nm apertures are opened in a layer of PMMA resist of thickness greater than 100 nm.

The patterned PMMA resist acts as a mask for the phosphorus-ion implant step to follow. The inset in figure 3b shows the result of a metallization and lift-off used to demonstrate the dimensions of these apertures. Following aperture definition, a 14 keV P+ ion beam is directed at the substrate to implant the donors. The PMMA layer is sufficiently thick to stop the ions and forward recoil of H atoms from the
PMMA itself, while ions which pass through the nano-apertures come to rest at a mean depth of 15 nm below the Si–SiO$_2$ interface and register a current pulse in the on-chip detector circuit. Following calibrated implantation and resist removal, the samples are then subjected to a 950 °C rapid thermal anneal (RTA) for 5 s to remove implant damage and activate the donors. The 5 s RTA process is necessary to limit P donor diffusion to ca. 1 nm.

Following ion implantation and activation, the remaining nanocircuitry on the surface of the chip is completed using two further EBL steps. Firstly, the Ti/Au control gates are deposited following EBL patterning of a single PMMA layer. The gates on the devices in figure 3, produced using this process, all have line widths below 20 nm and we have reliably demonstrated line widths of 12 nm with this process. Finally, the two Al/Al$_2$O$_3$ SETs are fabricated using a double-angle metallization process and a bilayer resist (Fulton & Dolan 1987). As seen in figure 3a, the overall alignment between all levels of this process is better than the width of a control gate (20 nm).

Preliminary electrical measurements on the device in figure 3a indicated that the two SET islands were more strongly coupled to each other than to the phosphorus donors below them. A new architecture has recently been developed to decouple the two SETs, and is shown in figure 3b. Here, the two SETs are separated by ca. 1 μm. However, each SET island is connected to the central donor region using a Ti/Au coupling electrode. These are designed to capacitively couple each SET to its target donor atom or atom cluster, but not to its neighbouring SET. To provide further isolation, a long barrier (B) gate is configured between the two donor clusters and SET couplers. Measurements on this device are currently underway.

3. Integrated quantum read-out with SETs

The practical read-out of a solid-state qubit is of central importance. For optimum performance, such a read-out device should be integrated with the qubit architecture. This suggests that one of the best measurement methodologies is to fabricate a solid-state device capable of electrical measurement of the qubit, with single-shot capability, fast response and robustness against noise. To that end we have concentrated on the SET (Grabert & Devoret 1992). This device is a highly sensitive electrometer, with performance close to the quantum noise limit. The SET has previously been identified as a key measurement device, not just for the Kane nuclear spin (Kane 1998; Kane et al. 2000; Pakes et al. 2003a) and electronic charge-based QCs (Hollenberg et al. 2003), but also for superconducting Cooper-pair box architectures (Aassime et al. 2001; Makhlin et al. 2001; Lehnert et al. 2003; Duty et al. 2003). Our work has focused on the study of twin-SET geometries, in which two aluminium-based SETs monitor the charge transfer in coincidence. This has the advantage of reducing sensitivity to spurious noise signals as the noise couples asymmetrically to each SET. Our work has been performed in both DC (Buehler et al. 2002, 2003a,b) and RF (Buehler et al. 2003c–e) modes of operation and is described below. We have also performed investigations of other SET geometries, including the double-island SET (Brenner et al. 2003), which offers the possibility of a completely different measurement device, and most recently we have begun to fabricate all-silicon SETs, which may offer lower noise levels.
Figure 5. (a) Schematic electrical circuit showing the twin-RF-SET circuit. (b) Upper trace: frequency dependence of the power reflected by the tank circuits, measured at the top of the dilution refrigerator. Lower trace: typical amplitude-modulation signal associated with each RF-SET measuring a signal corresponding to ca. 0.1 e at 2.5 MHz; (i) $\delta q_{\text{SET}1} = 7.5 \mu e \text{ Hz}^{-1/2}$, (ii) $\delta q_{\text{SET}2} = 4.4 \mu e \text{ Hz}^{-1/2}$. Horizontal arrows indicate the relevant y-axis. (c) Bias spectroscopy of the RF-SET. Reflected power is monitored as a function of gate bias and source–drain bias for each RF-SET, allowing the identification of the DJQP resonance which is the optimum working point for the RF-SET. (Reproduced from Buehler et al. (2003d).)

To demonstrate the correlated detection of electron tunnelling events, we constructed the aluminium nanostructure shown in figure 4. Here two metal ‘dots’, connected by an aluminium oxide tunnel junction, in the centre of the device, are used to simulate the P donors. The two adjacent SETs then detect single charge transfer between dot 1 and dot 2 when an electric field is applied across the dots by applying equal and opposite biases to gates A1 and A2. This double dot is thus a direct, but classical, simulation of an electronic charge qubit; as an electron is transferred from one metal island to the other, both SETs simultaneously register equal and opposite signals. Figure 4c shows the conductance of the SETs as a function of the electric field applied across the double dot. Electron transfer between the dots is clearly seen by the periodic simultaneous discontinuities in the outputs of the two SETs ($\Delta V = 31 \text{ mV}$), superimposed on top of the standard Coulomb blockade oscillations of each SET ($\Delta V = 68 \text{ mV}$). To show this more clearly, we use the G1 and G2 gates to keep the conductance of the SETs constant, so that only discrete events due to charge motion are detected (figure 4d).
Figure 6. (a) Upper trace: individual RF-SET responses to periodic charge transfer with four averages. Middle trace: correlation signal showing clear charge transfer. Lower trace: applied gate biases to induce charge transfer. (b) Upper trace: RF-SET responses without averaging. Charge noise can be seen affecting one of the SETs in the grey region but the correlation signal (lower trace) shows significant noise rejection. (Reproduced from Buehler et al. (2003e).)

The upper trace of figure 4d shows the SET conductance where the G gates (see figure 4a) have compensated for the effect of the A-gate potentials on the SETs and the lower trace shows the correlation signal. The correlation signal is obtained by taking the derivative of the SET conductances (generating the transconductance) and multiplying these together. By correlating in this fashion, we are able to reject charge noise events which are detected by one SET and not the other. This rejection can be clearly seen in figure 4d, where a random charge event has been detected by SET 1 but not SET 2. Although the transconductance for SET 1 shows a signal comparable in size with the previously measured charge transfer event, the correlation signal shows no such event. In this way we greatly enhance the read-out fidelity.

In addition to being able to distinguish real signal from noise, the read-out must occur on time-scales shorter than the qubit relaxation time $T_1$. For charge-based qubits, this is expected to be $0.1 - 10 \mu s$ (Hollenberg et al. 2003). Although spin qubits have much longer relaxation times ($T_1 \approx 100 \text{ ms}$ has been recently reported\(^\dagger\)), when the spin information is converted to charge information for SET-based read-out, a similar restriction may apply (Kane et al. 2000). By operating the SETs at radio frequencies, it is possible to greatly enhance the time-domain sensitivity (Schoelkopf et al. 1998), while retaining the extreme charge sensitivity. Therefore, we have developed a fast twin-RF-SET read-out scheme which allows correlated charge motion detection on microsecond time-scales, with spurious-signal rejection.

A schematic of the electrical set-up is shown in figure 5a, and is described in more detail elsewhere (Buehler et al. 2003d). In this circuit, each SET provides a

\(^\dagger\) E. Yablonovitch 2003, unpublished research, presented as ‘The electron spin in silicon, a promising qubit’ at US/Australia Workshop Solid State and Optical Approaches to Quantum Information Science, Sydney, Australia.

variable damping to an $LC$ resonator. By choosing different values of $L_1$ and $L_2$ we can tune the resonance of each SET to a different frequency (figure 5b), and monitor both SETs simultaneously. The upper trace in figure 5b is the reflected RF power from the tank circuit with no signal applied to the SETs, and the lower trace shows a typical signal when a 2.5 MHz signal is applied to a gate that couples equally to both SETs, inducing a charge of ca. 0.1e on each SET island. This lower trace allows us to calculate the sensitivities of the RF-SETs as 7.5 $\mu$e Hz$^{-1/2}$ and 4.4 $\mu$e Hz$^{-1/2}$. The theoretical charge sensitivity limit of a realistic, optimized RF-SET is 2 $\mu$e Hz$^{-1/2}$ (Devoret & Schoelkopf 2000), so our sensitivities are close to the fundamental limit. In order to achieve the optimum sensitivity, we tune our devices using the source–drain and gate biases to the double-Josephson-quasi-particle resonance (DJQP) (figure 5c), which theory suggests is the optimal configuration for a superconducting SET (Clerk et al. 2002). We next use these optimized SETs to detect single-electron transfer between the metal dots (figure 7) on microsecond time-scales. The bias applied to the A gates is now increased very rapidly (lower panel of figure 6a), which induces charge transfer between the metal dots. The top trace shows the response of the RF-SETs (as was shown in figure 4 for the DC-SETs); the simultaneous discontinuities in the output of the two RF-SETs indicate charge transfer events. The data clearly show periodic charge transfer with periodic peaks in the correlation (middle panel), since each trace is obtained by averaging four separate traces. The effects of charge noise become much more evident if each measurement is performed single shot, as is required for optimum for QC read-out (figure 6b). The upper SET trace in figure 6b now shows artefacts due to charge noise (highlighted in grey). However, the noise does not affect the correlation measurement (lower trace). Such results suggest that correlated RF-SETs are excellent candidates for performing fast, single-shot measurements on solid-state quantum computing architectures.

4. Bottom-up atomically precise phosphorus array fabrication

While ion implantation provides a rapid path for the study of few-qubit devices, there will always be some deviation in the position of the phosphorus donors from the ideal array sites resulting from the statistical nature of the implant process. This deviation should not be problematic for charge-based qubits but could introduce significant variations in exchange coupling between donors in the case of spin qubits. For atomic-scale precision in phosphorus donor placement a ‘bottom-up’ approach to fabrication is necessary. Figure 7 shows such a process which employs atomic-scale lithography of a hydrogenated silicon surface using a scanning tunnelling microscope (STM), together with silicon overgrowth via molecular beam epitaxy (O’Brien et al. 2001; Simmons et al. 2003). This technology provides a path towards atomically precise doping of a semiconductor, together with a methodology to construct large-scale precise Si:P qubit arrays. We review progress achieved to date on key steps in this approach.

The bottom-up fabrication process shown in figure 7a begins with preparation of a clean, defect-free Si(100) surface, followed by passivation using atomic hydrogen to form a monolayer (ML) of monohydride resist (step 1). An STM tip is then used to desorb single H atoms from the resist, thereby exposing the underlying Si substrate (step 2). During subsequent exposure of the surface to phosphine ($\text{PH}_3$) gas, single P-containing molecules only adsorb at the exposed regions of Si surface (O’Brien et
al. 2001) (step 3). Annealing at ca. 350 °C (step 4) then incorporates P atoms from the phosphine molecules into the Si surface, while leaving the hydrogen resist layer unaffected (Oberbeck et al. 2002; Curson et al. 2003a; Schofield et al. 2003). This step is critical. Prior to annealing, the phosphine molecules are weakly attached to the exposed silicon surface with one covalent bond. Following annealing, however, the incorporated P atoms form three covalent bonds to silicon atoms, securing the phosphorus atom in its patterned location by providing a stronger resistance to thermal diffusion.

The remaining steps in figure 7a involve encapsulation of the phosphorus array. In step 5, the hydrogen resist layer is removed from the surface without destroying the ordered array of phosphorus atoms. In step 6 the phosphorus atoms are then encapsulated by a few MLs of silicon grown at room temperature (RT) (Oberbeck et al. 2003). Subsequent rapid annealing (step 7) reduces the defect density in the silicon layer and flattens the surface. The last three steps involve further Si growth at higher temperatures to achieve the necessary Si-layer thickness of 5–20 nm, followed by growth of an insulating barrier layer and the registration of surface metal gates to the buried phosphorus atoms. We have already demonstrated steps 1–4 (O’Brien et al. 2001; Oberbeck et al. 2002; Curson et al. 2003a; Schofield et al. 2003), step 5 (unpublished) has recently been achieved and we are currently developing the final process steps.

Patternning of a hydrogen-terminated Si(001) surface was first demonstrated by Lyding et al. (1994), who used a highly confined electron beam generated by the tip of an STM to desorb hydrogen atoms, exposing the underlying Si surface. As shown in figure 8a,b, we have used this technique to perform controlled lithography using the STM tip to create both large areas (200 × 30 nm²) and parallel, nanometre-wide lines of bare Si. Large lithographically defined areas are used as registration markers for the relocation of atomic-scale features on the surface after process steps such as sample annealing. Figure 8c demonstrates atomic-precision single-atom lithography, where ultimate resolution is attained by pulsing the STM tip at ca. 1.5 nm intervals to desorb single H atoms, in this case from the right-hand side of five consecutive dimer rows (Schofield et al. 2003).

Following the demonstration of atomic-scale hydrogen lithography we have carried out an extensive series of STM experiments, summarized in figure 9, which demonstrate an ability to incorporate single phosphorus dopants in a silicon surface with atomic precision: step 4 in figure 7a.

The STM image in figure 9a shows an Si(001) surface after flash-annealing to 1200 °C, cooling to RT and dosing with 0.01 Langmuir (1 L = 0.75 × 10⁻⁶ mbar s) of PH₃ gas. Two adsorbed PH₃ molecules appear in this image as bright circular protrusions with an apparent height of ca. 0.07 nm above the substrate dimer rows (Schofield et al. 2003; Wang et al. 1994). A schematic of these adsorbed PH₃ molecules is shown in figure 9b. After a controlled anneal to 550 °C, the circular adsorbate protrusions are replaced by asymmetric features that have an apparent height of ca. 0.03 nm with respect to the substrate dimer rows, two of which are shown in figure 9c. These features are Si–P heterodimers (Curson et al. 2003a; Oberbeck et al. 2002), as indicated schematically in figure 9d. The Si–P heterodimer is formed by the substitution of a P atom with one atom of an Si dimer. The displaced Si atom is ejected onto the surface and at this anneal temperature has enough mobility to diffuse to a step edge, to which it bonds. Having developed an understanding of how PH₃ interacts

Figure 7. (a) Schematic of the ‘bottom-up’ fabrication process. (b) Key reactions known to occur on PH$_3$/Si(001) and H/Si(001) surfaces, as a function of annealing temperature. The processes shown are dissociation of PH$_3$ to form PH$_2$, dissociation of PH$_2$ and subsequent incorporation of P atoms into the surface layer, desorption of H atoms and finally desorption of P atoms.

with the clean Si(001) surface (Curson et al. 2003b), we have then used STM-based lithography to demonstrate that PH$_3$ molecules can be adsorbed on the surface with atomic precision.

Figure 9f shows an atomic-resolution STM image of three hydrogen desorption sites, ca. 3 nm apart, on an otherwise H-terminated Si(001) surface (O’Brien et al. 2001). The bright protrusion at each of the desorption sites is the signature of a single silicon dangling bond, after desorption of just one hydrogen atom. Figure 9g shows the same area of the surface after dosing with PH$_3$ at RT. The effectiveness of the hydrogen resist as a barrier to phosphine adsorption is demonstrated by the uniform hydrogen coverage after phosphine dosing except at the previously desorbed hydrogen sites. Analysis of line profiles (not shown) reveals a characteristic increase of ca. 0.05 nm in the height of the protrusion after phosphine dosing (O’Brien et al. 2001), which confirms the adsorption of a PH$_3$ molecule.

Figure 9h, i demonstrates the incorporation of an individual P atom into the silicon surface with atomic precision by the use of a critical anneal step. Figure 9h shows a hydrogen-terminated silicon surface with a controlled single desorption site around two to three dimers in length, created using the STM tip. Figure 9i shows the same
Figure 8. An STM tip has been used to remove hydrogen atoms from a hydrogen-terminated Si(001) surface to form (a) a 200 nm × 30 nm rectangular patch, (b) two parallel lines of bare Si(001) surface, and (c) five single hydrogen-atom desorption sites. The desorption parameters used were +4 V sample bias and 1 nA tunnel current. The areas of bare Si(001) surface appear brighter than the surrounding H-terminated surface, due to the additional tunnel current contributed by the Si surface states.

Figure 9. (a)–(e) STM images and schematics of the interaction of PH$_3$ with the Si(001) surface. (a) STM image and (b) schematic of an Si(001) surface, consisting of rows of paired Si atoms (dimers), and two molecularly adsorbed PH$_3$ molecules. (c) STM image and (d) schematic of a PH$_3$-dosed and annealed (ca. 550 °C) Si(001) surface showing two incorporated P atoms. (e) Schematic of an Si dimer and an Si–P heterodimer. STM images of three desorption sites of H-terminated Si(001) before (f) and after (g) phosphine dosing. (h), (i) STM images of atomically precise single P atom incorporation into the surface of H-terminated Si(001): (h) H-terminated Si(001) with a single H-desorption point; (i) the same area after PH$_3$ dosing and annealing to 350 °C showing that a single P atom has been incorporated at the location defined by the H-desorption point.
desorption site after PH$_3$ dosing with ca. 0.3 L PH$_3$ and annealing to 350 °C. We can clearly see the asymmetric H-Si–P heterodimer. In contrast to the clean-surface results, the Si–P heterodimers are hydrogen terminated as a result of the abundance of surrounding hydrogen, such that the silicon dangling bond is now hydrogen passivated and no longer protrudes from the surface. To our knowledge, this is the first demonstration of the controlled incorporation of a single dopant atom into a silicon surface (Schofield et al. 2003) and not only makes possible large-scale silicon-based QC devices (Kane 1998) but also opens up new possibilities for atomic-scale electronic devices such as classical single-atom memories (Snider et al. 1999).

Our ability to thermally incorporate phosphorus atoms into the silicon surface without disturbing the hydrogen resist is consistent with previous studies of phosphine-dosed Si(001) (Hamers & Wang 1996; Shan et al. 1996; Lin et al. 1999) and hydrogen-dosed Si(001) (Suemitsu et al. 1994) surfaces. Figure 7b summarizes these studies by showing the relevant reactions that are known to occur as a function of annealing temperature. From the figure we see that our 350 °C phosphorus-incorporation step exploits a natural temperature window in the surface chemistry of these adsorption systems.

Following formation of the P array in the Si surface, the next step of our process is the encapsulation in epitaxial Si. During this encapsulation process, the carefully created P array must be kept intact, with segregation and diffusion of the P atoms minimized by keeping the growth temperature as low as possible. We have studied P segregation and diffusion under different encapsulation and annealing conditions using the STM to image P atoms at the surface. We have also shown that the incorporation of P atoms into the Si surface via the annealing step results in electrical activation of the P atoms (Oberbeck et al. 2002). Annealing of the sample after low-temperature growth is necessary to flatten the surface and, for the purpose of monitoring the vertical segregation, identify the characteristic asymmetric appearance of the Si–P heterodimer, shown in figure 9c, e.

Figure 10a–f shows filled-state STM images taken at RT of two separate encapsulation experiments. For each experiment, STM images of the clean Si(001) surface are shown after: initial flashing; P incorporation; Si overgrowth at different temperatures; and successive annealing steps for 5 s at temperatures close to 350 °C, 500 °C and 600 °C. For compactness we show only selected STM images of the annealing sequence. The analysis of the data is summarized in figure 10g. The two experiments differ only in the Si overgrowth step: 5 MLs of Si were grown either at 255 °C (left column) or at RT (right column). After P incorporation and 5 MLs of Si growth, annealing of the surface at temperatures of 345 °C (figure 10d), 498 °C (figure 10e) and 600 °C (figure 10f) causes the Si surface to flatten due to island coarsening and diffusion of Si atoms to step edges. Simultaneously, the density of bright asymmetric features resulting from vertically segregated P atoms forming Si–P heterodimers at the surface increases. Figure 10d–f demonstrates that the density of Si–P heterodimers at the Si surface is much lower for a given anneal temperature if the Si encapsulation occurs at RT compared with 255 °C Si growth.

To quantify the density of P atoms at the Si(001) surface observed in the STM images in figure 10 the number of Si–P heterodimers was counted after each anneal. Figure 10g shows the increase in the relative density of P atoms at the surface following subsequent annealing steps for the two experiments. The relative density is obtained by comparison of the phosphorus density after Si growth and sample anneal-
ing with the initial density of incorporated phosphorus atoms after phosphine dosing of the clean Si surface. We first consider the results for encapsulation with 5 MLs of Si grown at 255 °C. After the first 5 s annealing step at the lowest applied annealing temperature (ca. 350 °C), already ca. 25% of the initial number of phosphorus atoms have segregated during Si growth and occupy surface lattice sites (see figure 10g). After subsequent annealing at 400, 450, 500, 550 and 600 °C, nearly 60% of the phosphorus atoms are present at the surface. These results demonstrate that even with encapsulation in epitaxial Si at relatively low temperatures (ca. 250 °C), a short low-temperature anneal results in significant segregation. In contrast, if phosphorus atoms are overgrown with 5 MLs of Si deposited at RT and annealed at 350 °C for 5 s, only ca. 5% of the initial number of P atoms are present at the surface. During the subsequent anneals, the P density increases only slightly to ca. 10%. This is a direct consequence of the strongly suppressed segregation of P atoms during Si overgrowth at RT. Looking forward, these experiments show that, to encapsulate phosphorus atoms in epitaxial Si with minimal segregation, not only should the Si growth temperature be as low as possible but more sophisticated and considerably faster anneal procedures will be necessary—for example, via the use of pulsed lasers of specific wavelength or other techniques.

In summary, the results presented above for the bottom-up approach show that considerable progress has been made towards fabricating a P array in Si for an Si-based QC. We have developed a process for incorporating single P dopants in Si with atomic-scale precision and have determined that, during Si encapsulation, P atom segregation/diffusion is minimized by RT growth followed by rapid annealing. We are currently in the process of combining these results to encapsulate a P array and characterize the spatial integrity of that array using buried dopant imaging. Also underway are studies of the barrier-layer growth between the embedded P array and surface electrodes and the process of accurately registering these electrodes to the buried qubits.

5. Conclusion

Solid-state approaches to quantum computing offer distinct advantages in terms of scalability and device integration. Furthermore, silicon-based approaches are compatible with technologies already used in conventional nanofabrication. The Kane approach is particularly attractive due to the extremely long coherence times for phosphorus nuclear spins in silicon. Our approach to the fabrication of a Kane QC begins with construction of the complementary Si:P charge qubit, for which read-out is achievable now using RF-SETs. Fabrication of the Si:P charge qubit is being approached via a ‘top-down’ method, employing single-ion implantation with on-chip detection, and a ‘bottom-up’ method, where advanced lithographic techniques are used to embed individual phosphorus atoms in silicon with atomic precision. Key targets for future work include: demonstration of the P-P+ charge qubit and measurement of qubit coherence times; in the bottom-up approach, integration of atomically precise phosphorus structures with surface control gates; and further optimizations of SETs to ensure quantum limited performance with optimal response times. Beyond Si:P charge qubits, spin-based qubits offer longer coherence times and commensurately greater prospects for scale-up and to this end electronic read-out of a single spin, compatible with the Kane architecture, is being pursued.
Figure 10. (a)–(f) Filled state STM images showing (a) the clean Si(001) surface, (b) the surface after phosphorus incorporation, (c) Si overgrowth, (d)–(f) annealing at various temperatures from two experiments: 5 MLs Si growth at 255 ºC (left column) and at RT (right column). STM images taken after various annealing steps show an increasing density of bright asymmetric features at the surface which are Si–P heterodimers. Image size of individual STM images is 50 × 25 nm². (g) Relative density of phosphorus atoms at the Si(001) surface after Si growth and various annealing steps. The density relative to the initial coverage was determined from STM images. The lines are a guide to the eye.

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