2D Materials for Electronics: Prospects and challenges

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Outline

- Introduction – the role of 2D materials for future electronics
- Structure and properties – graphene, transition metal dichalcogenides, and black phosphorus
- Synthesis
- 2D Devices – transistor and tunnel FET
- Conclusion
Family of 2-D Crystals

- More than 140 two-dimensional (2-D) materials, and the number is still growing
- Covering insulators, semiconductors, and metals

<table>
<thead>
<tr>
<th>Material</th>
<th>Structure</th>
<th>Bandgap</th>
<th>Mobility (cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Graphene</td>
<td><img src="image" alt="Graphene" /></td>
<td>0</td>
<td>1000-100,000</td>
</tr>
<tr>
<td>h-BN</td>
<td><img src="image" alt="h-BN" /></td>
<td>~7.2 eV (indirect)</td>
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<tr>
<td>TMD (MX₂)</td>
<td>M: W, Mo, Hf, Zr, Ti, Cr, Ta X: S, Se, Te</td>
<td>0.6 – 2.3 eV, and depending on layer #</td>
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Promises of 2D Materials
50 Years of Moore’s Law

Imagine fitting the entire China population in 10 original music halls – That’s the scale of Moore’s Law!

Source: Intel
50 Years of Moore’s Law: Can it be continued?

Need innovation for each generation below 10 nm!

Strained Si (2003)

High-k Metal Gate (2008)

FinFET (2011)

IEEE Spectrum Nov. 2011, p50
The Major Issue is Leakage

Electrostatic Length

Body thickness


The transistor becomes more difficult to “Turn Off” as the gate dimension shrinks.

No leakage control, no scaling!
Scaling Issue for 3D Materials

- Electrostatic length \( \lambda = \sqrt{t_s t_{OX} \varepsilon_s / \varepsilon_{OX}} \)

- \( L \approx 5 \lambda \) to suppress short-channel effect (SCE)

- Severe mobility degradation for body thickness < 5nm

* Double gate with EOT = 0.8 nm, \( L = 5 \text{nm} \)

<table>
<thead>
<tr>
<th>Materials</th>
<th>Dielectric Constant</th>
<th>Body Thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>11.7</td>
<td>0.82</td>
</tr>
<tr>
<td>Ge</td>
<td>16.2</td>
<td>0.58</td>
</tr>
<tr>
<td>GaAs</td>
<td>12.9</td>
<td>0.74</td>
</tr>
</tbody>
</table>

Less than 1nm!!

DIBL: Drain-Induced Barrier Lowering
2D: Ultra-thin Channel with Good Mobility

2D materials could exhibit high mobility values for sub-nm thickness!
Fundamental Properties of (selected) 2D Materials
## Family of 2-D Crystals

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Graphene: Lattice and Band Structure

Lattice structure

- Two carbon atoms per unit cell

- Massless fermion

- Linear E(k) dispersion

- Zero bandgap due to inversion symmetry

In-plane sp2 covalent bond

Band structure
2-D Transition Metal Dichalcogenide

- Lattice structure (1H)
  
  **Top view**

- Band structure of MoS$_2$
  
  - 4 Layer
  - 3 Layer
  - 2 Layer
  - 1 Layer

- Direct gap at monolayer
- Indirect gap with smaller $E_G$ at few layers
- Weak interlayer bonding by van der Waals forces

M = Transition metal (Mo, W, etc.)
X = Chalcogen (S, Se, Te)

Splendiani et al., *Nano Lett.* 10, 1271 (2010)
Direct to Indirect Gap in TMD - Layer dependence

10^4 times stronger photoluminescence (PL) in 1 layer MoS_2

A. Splendiani et al., Nano Lett. 10, 1271 (2010)
K. F. Mak et al., PRL 105, 135805 (2010)
Black Phosphorus - Phosphorene

- Lattice structure – puckered honeycomb

- Band structure

- Direct gap (ML to bulk)
- $E_G = 0.3 eV$ for bulk, and $2.0 eV$ for ML
- Highly anisotropic effective mass in $x$ (light) and $y$ (heavy) for both electron and holes
Synthesis of 2D Materials
Carbon in All Dimensionalities

Graphene (2D)

Graphite (3D)

Nanotube (1D)

Fullerene (0D)
How to Make Graphene?
Or, Try This at Home …

You may win one of these ten years ago....

Also works for other 2D Materials!
Large-Area Graphene Growth by CVD

CH$_4$ \rightarrow C \rightarrow C \rightarrow \sim 600^\circ \text{C} \rightarrow C \rightarrow C \rightarrow C

Metal (Ni, Cu, Ru, etc)

Cool down

SEM of CVD graphene on Cu

Metal (Ni, Cu, Ru, etc)
Low-Cost Graphene Production

CVD growth

Electrochemical delamination

Clean copper and reuse

GRAPHENE TRANSFER
Large-Area Graphene Production

2005

2009 - 2010

2012

2013 ~

~5 μm

~50 cm

~1 m

~ 10m

~60 inch
Scalable Synthesis of MX\textsubscript{2}

**MoS\textsubscript{2} by MoO\textsubscript{3}/S CVD at 700°C**

\[ \text{carrier gas} \rightarrow \text{MoO}_3, \text{S} \rightarrow \text{MoS}_2 \text{ on substrate} \]

van der Zande et al., Nat. Mater. 12, 554 (2013)

**MoS\textsubscript{2} by thermolysis at 1000°C**

\[ (\text{NH}_4)_2\text{MoS}_4 \text{ solution} \rightarrow \text{S}_2 \text{ on sapphire} \]


**Sulfurization of sputtered metal**


Challenge – how to maintain Mo:S = 1:2?
Synthesis of Black Phosphorus

BP by transport reaction at 650°C

Raman Spectra of Synthesized BP

Challenges – Breakthrough to achieve direct synthesis of thin-film BP on substrate!

M. Kopf et al., J. Cry. Gro. 405, 6 (2014)
Status of 2D Materials Synthesis

- A number of growth methods to produce large-area TMD films on various substrates (oxide, metal) are available.

- Top-down growth of phospherene is yet to be demonstrated.

Fiori et al., Nat. Nano. 9, 768 (2014)
2D Electronics
Graphene Technology Roadmap

K.S. Novoselov, et. al; A roadmap for graphene; Nature, Vol 490,(2012),192

- Graphene Technology Roadmap
  - Graphene Transfer (Medium Quality)
    - Touch screen
    - Rollable E-paper
    - Foldable OLED
  - Transferred or Directly Grown Large Area Graphene (High Quality)
    - RF Transistor
    - Logic Transistor/TFT
  - Future Devices

- Flexible and Rigid
  - Graphene touch panel

- Rollable Display

- Graphene FET and Circuits
Graphene vs. bulk Semiconductors

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>In_{0.53}Ga_{0.47}As</th>
<th>InAs</th>
<th>InSb</th>
<th>Graphene</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron mobility (cm²/Vs) at n = 10^{12} cm⁻²</td>
<td>600</td>
<td>4,600</td>
<td>7,800</td>
<td>20,000</td>
<td>30,000</td>
<td>25,000 (flake)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>~3000 (Epieaxial)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>~2000 (CVD)</td>
</tr>
<tr>
<td>Electron saturation velocity (10⁷ cm/s)</td>
<td>1</td>
<td>1.2</td>
<td>0.8</td>
<td>3.5</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>Ballistic mean free path (nm)</td>
<td>28</td>
<td>80</td>
<td>106</td>
<td>194</td>
<td>226</td>
<td>400</td>
</tr>
<tr>
<td>Band-gap (eV)</td>
<td>1.12</td>
<td>1.42</td>
<td>0.72</td>
<td>0.36</td>
<td>0.18</td>
<td>0</td>
</tr>
</tbody>
</table>

Key features

- A true two-dimensional system
- Ambipolar transport
- Optically transparent
- Flexible with high mechanical strength
- Zero bandgap
Graphene Field-Effect Transistor (FET)

- Poor on/off ratio
- Bad for digital switches

Current [uA] vs. Voltage [V] gate (Vg)

- Dirac point
- V_d = 0.1 V

Dos hole electron

D.O.S electron

source graphene drain

Back gate

S D S D

graphene

- D.O.S

Poor on/off ratio
Bad for digital switches
Graphene for RF electronics

High on/off ratio is not required for RF applications.

\[ g_m = \frac{\Delta I}{\Delta V_g} \]

\[ f_T : \text{cut-off frequency where current gain is 1} \]

\[ f_T = \frac{g_m}{2\pi C_g} \]
GHz Graphene Device and Circuit

Lin et al., Science 327, p. 662 (2009)

100-GHz Transistors from Wafer-Scale Epitaxial Graphene

Y.-M. Lin,* C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, Ph. Avouris*

Gate length: 240 nm
\( f_T : 60 \text{ – } 100 \text{ GHz} \)

Gate length: 550 nm
\( f_T : 25 \text{ – } 50 \text{ GHz} \)
GHz Graphene Device and Circuit

Lin et al., Science 332, 1294 (2011)

Wafer-Scale Graphene Integrated Circuit

Yu-Ming Lin,* Alberto Valdes-Garcia, Shu-Jen Han, Damon B. Farmer, Inanc Meric,† Yanning Sun, Yanqing Wu, Christos Dimitrakopoulos, Alfred Grill, Phaedon Avouris,* Keith A. Jenkins

Lin et al., Science 332, 1294 (2011)
Beyond 400 GHz Operation

**LETTER**

Nature 472, 74 (2011)

doi:10.1038/nature09979

High-frequency, scaled graphene transistors on diamond-like carbon

Yanqing Wu¹, Yu-ming Lin¹, Ageeth A. Boï², Keith A. Jenkins¹, Fengnian Xia¹, Damon B. Farmer³, Yu Zhu¹ & Phaedon Avouris¹

PNAS 109, 11588 (2012)

Nanowire Gate ~ 40 nm
427 GHz (UCLA)

Lg = 40nm
350 GHz (IBM)

High-frequency self-aligned graphene transistors with transferred gate stacks

Rui Cheng¹*, Jingwei Bai¹*, Lei Liao, Hailong Zhou, Yu Chen, Lixin Liu, Yung-Chen Lin, Shan Jiang, Yu Huang, and Xiangfeng Duan¹*²

*Departments of Materials Science and Engineering, and *Chemistry and Biochemistry, and °California Nanosystems Institute, University of California, Los Angeles, CA 90095
Creating a Bandgap in Graphene

\[ E_g \sim 1.4 \text{eV/W}, \text{(Width in nm)} \]

Graphene Nanoribbon

- Edge roughness
- Width variation

Challenge-
Atomically smooth edge with a precise width control

Han et al, Phys. Rev. Lett. 98, 206805
Choice of 2D Material for CMOS

Ling et al., PNAS 112, 4523 (2014)
Short-Channel MoS$_2$ FET - Good switching down to 11nm

Nourbakhsh et al. (2015 VLSI Symp.)

\[ \lambda = \frac{1}{N} \epsilon_S t_S \frac{t_{OX}}{\epsilon_{OX}} \], \text{ N=2 for double gate}
Phospherene p-FET

Xia et al., Nature Comm. 5, 4458 (2014)
Stability of Phosphorene in Air

BP disintegrates in ambient.

B. Ozyilmaz et al., Nature Comm. 6, 6647 (2015)

Passivation with BN

Chen et al., Nature Comm. 6, 7315 (2015)
Issues of Contacts in 2D Materials

- Schottky barrier and Fermi-level pinning
- Currently achievable Rc for TMDs and BP are still two orders of magnitude higher than Si and ITRS requirement

<table>
<thead>
<tr>
<th>Transistor type</th>
<th>$R_c$ (Ω mm)</th>
<th>Metal</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Graphene MOSFET</td>
<td>0.011–0.08</td>
<td>Ni, Ti</td>
<td>BL</td>
</tr>
<tr>
<td></td>
<td>0.1–0.2</td>
<td>Ti, Ni, Pd/Au, Cr/Au</td>
<td>SL</td>
</tr>
<tr>
<td>MoS$_2$ MOSFET</td>
<td>0.2–1.6</td>
<td>Ni/Au, Ti/Au, Au</td>
<td>FL</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Graphene</td>
<td>BL</td>
</tr>
<tr>
<td>WSe$_2$ MOSFET</td>
<td>1.4</td>
<td>Graphene</td>
<td>FL</td>
</tr>
<tr>
<td>Phosphorene MOSFET</td>
<td>1.75</td>
<td>Ni/Au, PdAu</td>
<td>FL</td>
</tr>
<tr>
<td>Si MOSFET</td>
<td>&lt;0.01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>InP HEMT</td>
<td>0.03</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GaAs mHEMT</td>
<td>0.02</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*ITRS 2024 requirement: $R_c = 0.065 \Omega \text{mm}$*

F. Schwierz et al., Nanoscale 7, 8261 (2015)
Tunnel FET: Low voltage operation

MOSFET with n/i/n junction

Tunnel FET with n/i/p junction

$\Delta V = 60\text{mV}, \frac{I_A}{I_B} = 1/10$

Thermal tail is filtered by bandgap and thus is not limited to 60mV/dec as in MOSFET
Tunnel FET vs. MOSFET

Lower operating voltage → lower power consumption!
Tunnel FET based on TMDs

From tunneling consideration:
1. Direct bandgap
2. Small mass in transport direction
3. Bandgap ~ 0.6eV

Appenzeller et al., IEEE XCDC (2015)
Comparison of TFET Performance

A. Seabaugh et al., J. EDS 2, 44(2014)
2D Candidates for TFET

Multilayer BP is also promising:
- Bandgap < 1eV
- Highly anisotropic carrier mass \( m_x << m_y \)
- Direct bangdap

<table>
<thead>
<tr>
<th></th>
<th>MoS\textsubscript{2}</th>
<th>MoSe\textsubscript{2}</th>
<th>MoTe\textsubscript{2}</th>
<th>WS\textsubscript{2}</th>
<th>WSe\textsubscript{2}</th>
<th>WTe\textsubscript{2}</th>
<th>BP 1L</th>
<th>BP 3L</th>
<th>BP 5L</th>
</tr>
</thead>
<tbody>
<tr>
<td>( m_{hx}/m_0 )</td>
<td>0.64</td>
<td>0.72</td>
<td>0.75</td>
<td>0.43</td>
<td>0.5</td>
<td>0.3</td>
<td>0.15</td>
<td>0.15</td>
<td>0.14</td>
</tr>
<tr>
<td>( m_{hy}/m_0 )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>6.35</td>
<td>1.12</td>
<td>0.89</td>
</tr>
<tr>
<td>( E_g ) (eV)</td>
<td>1.68</td>
<td>1.51</td>
<td>1.085</td>
<td>1.93</td>
<td>1.56</td>
<td>0.75</td>
<td>1.53</td>
<td>0.73</td>
<td>0.52</td>
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Vertical Tunnel FET with 2-D Materials

- Stacking of n- and p-type 2D crystals
  - Enhanced tunnel area
  - Ultra-short junction

Gong et al., Appl. Phys. Lett. 103, 053513 (2013)
2D Heterojunction Vertical TFET

T. Roy et al., ACS Nano 9, 2071 (2015)
Tunnel FETs are promising for better EDP than Si MOSFETs.
Conclusion

- 2D materials have potential for future electronics
  - The real and unique benefits is the atomically thin body

- So far, experimental studies have yet to demonstrate the full advantage and potential of 2D materials for electronic devices
  - Short history of only ~4 year for TMDs and ~1 year for BP

- Materials synthesis will be one deterministic factor
  - Most 2D materials in their bulk form has been extensively used in industrial applications
  - Defect density?

- Other fundamental challenges
  - Contact resistance
  - Doping scheme
  - Gate stack options
Thank you